

(3 Hours)

[Total Marks: 80]

N.B : (1) Question No.1 is compulsory.

(2) Attempt any three questions from remaining questions.

(3) Figures to the right indicate full marks.

Q1) Answer any Four

20

- What are the different Types of Tasks in a Real Time System? Give suitable Examples.
- Differentiate between SPI and I2C Bus.
- Give the significance of Watch Dog Timer for a given application.
- Explain the Design Metrics of an Embedded Systems.
- Draw the Data flow Graph for

$$y = \sqrt{a^2 + b^2} \quad \text{and} \quad z = \frac{(ab+cd)}{2}$$

Q2) a) Explain the CAN Bus Protocol. How it is suitable for Real Time applications. 10

b) Explain the Task State Diagram. What is a Task Control Block.? 10

Q3) a) What is Priority Inversion, Unbounded Priority Inversion .

Give the Solution to overcome it. 10

- b) Give the Utilization bound for Rate Monotonic Scheduling Algorithm and find if the following Task Set is $T_i(e_i, P_i)$ RMA schedulable.

Show using Time Line Diagram. $T_1: (1,4)$, $T_2(2,5)$ $T_3(5,20)$ 10

Q4) a) What type of Real Time System is a “Air Bag Deployment Unit in a Car.”. 10

Write suitable PseudoCodes using MicroCOS/II functions OSInit(), OSStart(), OSFlagCreate(), OSFlagPost() OSFlagPend().

Consider **Task1**: Detects Accident

Task2: Deploys Air bag on detection of Accident. Explain the operation of each

MicroCOS/II function used.

- b) Explain the Earliest Deadline First Scheduling Algorithm. State its Advantages and Disadvantages. 10

Q5) Design a Automatic Chocolate Vending Machine.Support the Design using 20

- a) Requirements b) Specifications c) Hardware /Software Architecture
- e) Testing /Debugging and System Integration.
- f) Use suitable MicroCOS/II functions.

Q6)Write Short Notes on **any 2** 20

- a)White Box and Black Box Testing, On chip Debugging.
- b)Hardware Software Co-Design Issues
- c)OSTaskCreate(),OSQPost(),OSQPend(),OSSemPost(),OSSemPend()
- d)Bluetooth /Zigbee
- e)Sensors and Actuators

Time: 3 hours

Marks: 80

N.B.

- 1) Question number ONE is compulsory.
- 2) Attempt any THREE questions from remaining questions.
- 3) All questions carry equal marks.
- 4) Figures to the right indicate full marks.

Q1

- a) What is meant by Umbrella Cell and Micro Cell in cellular systems? 5
- b) Explain authentication and security in GSM 5
- c) Differentiate between soft hand off and hard hand off 5
- d) Differentiate between CDMA, TDMA and FDMA 5

Q2 a) A total of 36 MHz of bandwidth is allocated to a particular frequency division duplex cellular telephone system, which uses two 25KHz simplex channels to provide full duplex voice and control channels. Compute the number of channels available per cell, if the system uses,

- a. 7-cell reuse and 10
- b. 12-cell reuse 10

b) Explain dynamic channel assignment strategy in a cellular system. What are the advantages of this scheme? 10

Q3 a) Explain with block diagram the Ground Reflection (two-ray) model of radio wave propagation. 10

b) Explain the difference between DSSS and FHSS with suitable block diagram. Which of the two is more bandwidth efficient? 10

Q4 a) Draw and explain the architecture of GSM. 10

b) Explain authentication process in a GSM system. What is the significance of white, grey and black registers? 10

Q5 a) Explain forward and reverse channels of IS 95. 10

b) Explain UMTS network architecture in detail with interfaces 10

Q6 Write short notes on **any 2** 20

- a) GPRS
- b) Hand of procedure in GSM
- c) Erlang B and Erlang C system
- d) Wireless sensor Networks

(3 Hours)

[Total Marks: 80]

- N.B.:
- (1) Question No. 1 is compulsory.
 - (2) Solve any three questions from remaining five questions.
 - (3) Draw neat diagrams and assume suitable data wherever necessary. Justify your assumptions.

1. Attempt any **four**: **20**
 - (a) Explain the four levels of addresses used in computers.
 - (b) Coaxial cable is much less susceptible to interference and cross talk than twisted pair. Why?
 - (c) What is sliding window? Where is it applicable?
 - (d) Explain leaky bucket to control congestion in network traffic.
 - (e) Identify the class of each addresses.
i)14.23.120.8 ii)252.5.15.111 iii)200.58.20.165 iv)128.167.23.20 v) 205.16.37.32
2. (a) Draw the OSI layer architecture. Explain the function of each layer and show the path of actual and virtual communication between the layers. **10**
 - (b) What is a transparent bridge? How the process of learning in this bridge takes place. Explain the Spanning tree algorithm to solve looping problem. **10**
3. (a) Explain Persistence methods with neat diagram. **04**
 - (b) Explain CSMA/CD with a flow diagram. **06**
 - (c) What are the two common configurations used in HDLC? Draw and explain the HDLC frame format with separate diagram for control field format for each different frame. **10**
4. (a) Compare Stop and Wait, Selective Repeat and Go-Back-N protocols for a noisy channel **10**
 - (b) Compare Circuit Switching, Packet Switching and Message Switching **10**
5. (a) List three transition strategies to move from IPV4 to IPV6. Explain the difference between tunneling and dual stack during transition period. **10**
 - (b) What is Fragmentation in IPV4? Explain the fields related to fragmentation in head format. **06**
 - (c) Find the first addresses, last addresses and number of addresses of the following IP addresses:- i) 205.16.37.39/28 ii) 123.56.77.29/27 **04**
6. Write Short note on (**any four**) **20**
 - i) DSL
 - ii) FDDI
 - iii) TCP header format
 - iv) Distance Vector Routing
 - v) Congestion Control

Time: 3 Hrs

Marks: 80

- 1) Question No.1 is compulsory.
- 2) Attempt any three question out of remaining five questions.
- 3) Assume suitable data whenever necessary.

- 1)
 - a) Represent $(78)_{10}$ and $(0.6125)_{10}$ in single precision floating point. 05
 - b) Explain basic structure of 4 stage Pipeline. 05
 - c) List Different I/O Access Methods. Explain any one detail. 05
 - d) Differentiate between SRAM and DRAM. 05

- 2)
 - a) Explain in detail organization of Cache Coherent – Non Uniform Memory Access. 10
 - b) What are the different types of pipeline Hazards. 10

- 3)
 - a) Explain Restoring Division algorithm and Perform $(14) \div (6)$ using it. 10
 - b) What is necessity of replacement algorithm? Show how pages are replaced between cache and main memory using replacement policies: 10
 - i) LRU
 - ii) FIFO
 - iii) LFU

- 4)

Explain Set Associative Mapping. Draw and explain a two-way set-associative mapping for cache that has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. 20

- 5)
 - a) What is micro programmed control? Explain in details. Write microinstruction for $MOV R_0, [R_1]$. 10
 - b) Describe Flynn’s Classification for parallel computer architecture. 10

- 6) Write Short Notes on
 - a) Superscalar Architectures. 10
 - b) Memory segmentation 10

77716