Time: 2 hour 30 minutes

Max. Marks: 80

Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1	The people who are entitled to apply for the registration of the copyright are
Option A:	assignee and licencee
Option B:	Author or artist
Option C:	Composer & producer
Option D:	All above
1	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
2.	Sectionprovides the inventions which are not patentable under the patent Act.
Option A:	Section 3 & 4
Option B:	Section 5
Option C:	Section 20
Option D:	All above
•	
3.	Which of the following is not an instrument of IPR?
Option A:	copyright 2 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5
Option B:	Land record
Option C:	Patents 255 CENTRAL PROPERTY OF THE PATENTY OF THE
Option D:	Trademarks 85 75 0 75 0 75 0 75 0 75 0 75 0 75 0 7
•	V. 434549V. C. X.
4.	The description of Patent is called
Option A:	Draft Second Sec
Option B:	Specification
Option C:	Assignment
Option D:	License
•	9.43.88.89.68.889.68.88.88.43.
5	The infringement of copyright may attract punishment with fine which may extend up to
Option A:	Rs 2 Lac to 3 Lac
Option B:	Rs. 10 Lac
Option C:	Rs. 50000 to Rs 2 Lac
Option D:	Rs 1 Crore
6.	The patent right gives an exclusive right to the patent to gain out of his
	invention.
Option A:	Monitory benefit
Option B:	Personal benefit
Option C:	Reputation in society
Option D:	All above
12,000	
7007	What protects the intellectual property created by Poetry writer?
Option A:	copyright
Option B:	Registered designs
Option C:	Patents
Option D:	Trademarks
87.500,00	
8.50	The new requirement for the patentable of the invention is
Option A:	Marketable
Option B:	Non obivious
Option C:	Profitable
7 / / <b>1</b> / / / / / / /	Inventive steps
Option D:	

9.	Trademark is used for	£ 4 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6
Option A:	It identifies the product and its origin	
Option B:	Earning the money from rent	
Option C:	Keeping business secrete	
Option D:	All above	625,45,7,488,5,48
10.	The term of patent shall be ye	ears 888888888888888888888888888888888888
Option A:	10	4 6 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8
Option B:	30	
Option C:	2-3	14 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
Option D:	20	

Q2	Solve any Two Questions out of Three 10 marks each
A	Discuss filling of Patents through PCT route
В	With the help of example explain in detail Patentable and non-patentable inventions
С	List out the purposes for which fair use of copyright work is permitted

Q3	Solve any Two Questions out of Three 10 marks each
A	What is copyright? Give the remedies for the infringement of copyright.
В	What is GI? List down prohibited GI in India.
C	Explain Multilateral treaties where India is a member (ex. TRIPS agreement, Paris
C	convention)

Q4	Write short notes on any two Questions out of three	10 marks each
A	Patent Litigation process	
В	WIPO O CONTROL OF CONT	
С	PCT SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS	

#### **University of Mumbai**

## Examination Second Half 2021 under cluster \_\_(Lead College: \_\_\_\_)

Examinations Commencing from 27th June 2022 to 14th July 2022

Program: M.E (Electronics)
Curriculum Scheme: Rev2019
Examination: ME Semester I

Course Code: **ELXDLO2021** and Course Name: **Advanced processor Architecture II**Time: 2hour 30 minutes

Max. Marks: 80

Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	Pentium 4 has how many caches?
Option A:	
Option B:	L1, L2
Option C:	
Option D:	L1, L2, L3
	900888888888888XX
2.	PCI has transfer rate of?
Option A:	130 Mbytes/sec
Option B:	135 Mbytes/sec
Option C:	132 Mbytes/sec
Option D:	140 Mbytes/sec
	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
3.	Way in which the components are interrelated is known as,
Option A:	function
Option B:	structure
Option C:	states 000000000000000000000000000000000000
Option D:	tasksVXXXXXX
825	1950 0 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8
4. 7.8	MAR refers as,
Option A:	Memory data register
Option B:	Memory Register
Option C:	Memory Counter
Option D:	Memory Address Register
	15 15 7 7 8 8 15 7 8 8 15 7 8 8 15 7 8 8 15 15 15 15 15 15 15 15 15 15 15 15 15
5.00	MIPS rate of a processor is given by
Option A:	
Option B:	f/10^6 X X X X X X
Option C:	f/CPI
Option D:	f/CPI x 10^6
506.00	Arbitration of PCI bus happens with,
Option A:	REQ#
Option B:	GNT #
Option C:	LOCK#
Option D:	REQ # and GNT # signals
\$7.4.5°	
087.78	Cache memory is divided into number of

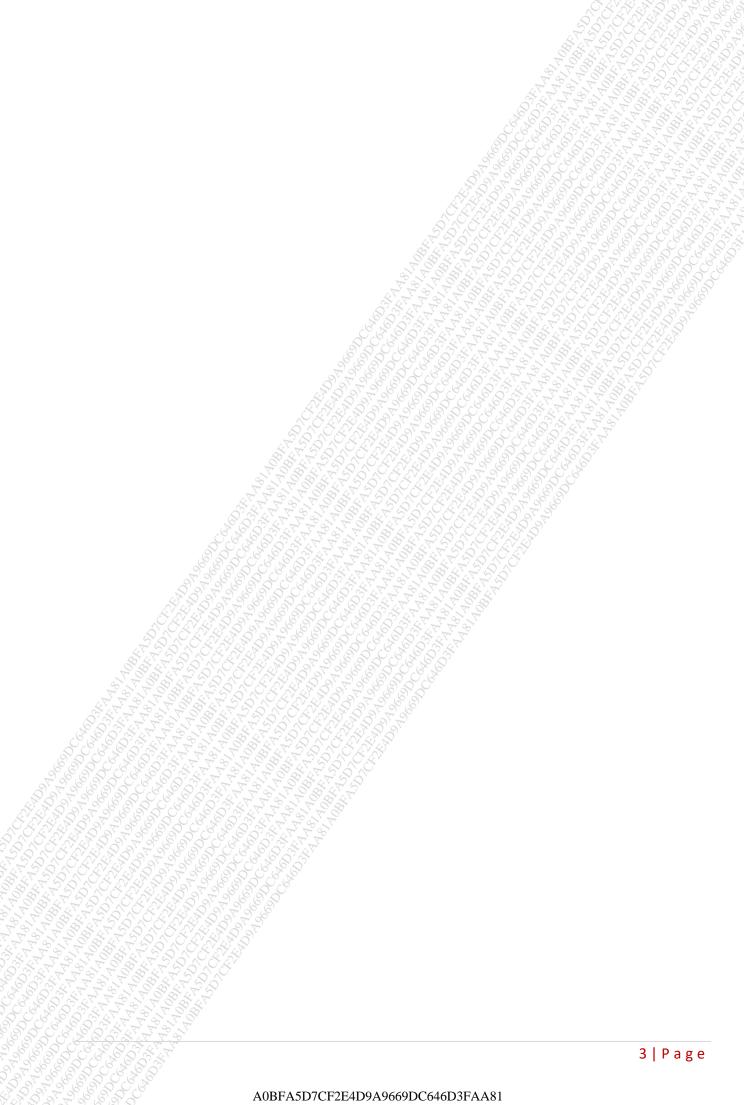
Option A:	blocks
Option B:	lines
Option C:	words
Option D:	units
	\$\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
8.	List the order of computer function
Option A:	data processing, data storage, control, data movement
Option B:	data processing, data storage, data movement, control
Option C:	data storage, data processing, data movement, control
Option D:	data processing, data movement, control, data storage
	Z 2 8 8 Z 2 D X 8 Z 2 D X 8 Z 2 Z 2 Z 2 Z 2 Z 2 Z 2 Z 2 Z 2 Z 2 Z
9.	Computer top level structure consists of,
9. Option A:	Computer top level structure consists of, CPU, Memory, I/O, Interconnection
Option A:	CPU, Memory, I/O, Interconnection
Option A: Option B:	CPU, Memory, I/O, Interconnection I/O, CPU, Interconnection, Memory
Option A: Option B: Option C:	CPU, Memory, I/O, Interconnection I/O, CPU, Interconnection, Memory CPU, I/O, Memory, Interconnection
Option A: Option B: Option C:	CPU, Memory, I/O, Interconnection I/O, CPU, Interconnection, Memory CPU, I/O, Memory, Interconnection
Option A: Option B: Option C: Option D:	CPU, Memory, I/O, Interconnection I/O, CPU, Interconnection, Memory CPU, I/O, Memory, Interconnection Memory, I/O, Interconnection, CPU
Option A: Option B: Option C: Option D:	CPU, Memory, I/O, Interconnection I/O, CPU, Interconnection, Memory CPU, I/O, Memory, Interconnection Memory, I/O, Interconnection, CPU Redundancy through hamming code is maintained in
Option A: Option B: Option C: Option D:  10. Option A:	CPU, Memory, I/O, Interconnection I/O, CPU, Interconnection, Memory CPU, I/O, Memory, Interconnection Memory, I/O, Interconnection, CPU  Redundancy through hamming code is maintained in RAID 1

# Please use either of the 3 option given below while setting up the subjective/descriptive questions

Q2.	Solve any Two Questions out of Three 10 marks each
A	Draw timing diagram of PCI read transfer and explain the same?
$\mathbf{B}$	Explain main features and functions of operating system?
\$ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Draw and explain Application Specific Adaptable Core Architecture with example?

Q3.	Solve any Two Questions out of Three 10 marks each
	Explain RAID and it's types with neat diagram?
B B B	Explain Micro architectural concepts in detail?
0,4,5,6,6, <b>C</b> 5,0,6,6,6	Explain the features of VLIW? Explain pitfalls in VLIW architecture?

$\mathbf{Q4}$	Solve any Two Questions out of Three 10 marks each
7.7.5.5.A.7.5.5.8.8	Explain reconfigurable architecture with an example? State its
	characteristics and applications?
B. 0. 0. 0. 0. 0. 0. 0. 0. 0. 0. 0. 0. 0.	Differentiate between Domain specific processors and Application
4574335743350	specific
17 4 8 5 4 5 8 6 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	Processors?
CT SO	Explain PCI master slave configuration in detail?



# University of Mumbai Examinations Summer 2022

Program: **Electronics Engineering**Curriculum Scheme: Rev 2016
Examination: ME Semester II

Course Code: ELXC2023 Course Name: Advanced Signal Processing

Time: 2 hour 30 minutes Max. Marks: 80

Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks (20 marks)	
1.	In direct form realization for an interpolator, which among the following generates an intermediate signal?	
Option A:	Upsampler	
Option B:	Downsampler	
Option C:	Anti-imaging filter	
Option D:	Anti-aliasing filter	
	\$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$	
2.	Analysis filter banks are used for	
Option A:	Separating a signal to several frequency bands(subband signals)	
Option B:	combining the processed subband signals to one signal	
Option C:	removing the noise in the signal	
Option D:	removing the image frequencies	
3.	Step size control which of the following parameters in an adaptive systems using LMS algorithm	
Option A:	Coefficients in adaptive filter	
Option B:	Speed of convergence	
Option C:	Energy spectrum	
Option D:	Power of signal	
200000000000000000000000000000000000000	7 8 8	

4.	The linear filter is an all pole filter is known as
Option A:	Autoregressive (AR) process
Option B:	Moving average (MA) process
Option C:	Autoregressive moving average (ARMA) process
Option D:	Parallel Process
5.	Wiener-Hopf equation is given by
Option A:	$W_{opt}$ =R+P
Option B:	$W_{opt}$ =RP
Option C:	$W_{opt}=RP^{-1}$
Option D:	$W_{\text{opt}}=R^{-1}P$
1	11 obt—17 1
6.	The estimate of power spectrum of random process is called
Option A:	Periodogram
Option B:	Energy spectrum
Option B.	Lifety spectrum
Option C:	Autocorrelation
Option D:	Expected value
	\$\circ
7.	The heart rate in ECG signals is computed using interval.
Option A:	R-R interval
Option B:	S-S interval
Option C:	T-T interval
Option D:	Q-Q interval
97597	88442076554522458
8.95	The speech signal is obtained after
Option A:	Analog to digital conversion
Option B:	Digital to analog conversion
Option C:	Modulator
Option D:	Demodulator
9.	Sampling is necessary
Option A:	In complex control systems
Option B:	Where high accuracy is required
Option C:	Non automated control systems
Option D:	Automated control systems

	4,4,4,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6,6
10.	Which of the following use quadrature mirror filters?
	\$60000 7 7 7 8 8 5 7 V
Option A:	Sub band coding
	6,8,0,0,8,0,0,8,0,0,0,0,0,0,0,0,0,0,0,0,
Option B:	Trans-Multiplexer
	\$\tag{2}\
Option C:	Sub band coding and Trans-Multiplexer
Option D:	Trans-Demultiplexer

Q2.	Solve any two out of the given three questions. All the sub questions carry 10 marks each .Total marks for this question is 20 marks (20)	
A	Explain applications of DSP in biomedical signal processing	
В	Derive the innovations representation of a stationary random process.	
С	Explain the LMS Algorithm with equations,	

Q3.	Solve any two out of the given three questions. All sub questions carry 10 marks each .Total marks for this question is 20 marks (20)
A	Explain the theory of parametric method of Power estimation.
В	Explain briefly forward linear prediction and draw the schematic of a prediction error filter.
С	Explain the applications of DSP in speech processing.

Q4.	Solve any two out of the given three questions. All the sub questions carry 10 marks each .Total marks for this question is 20 marks (20)
8 7 A 7 5 6	Describe any 3 properties of Linear prediction error filter.
B	Explain decimation process with a block diagram. Draw the spectral diagrams of the input and output signals.
856 XC358	Explain the Blackman and Tukey method of smoothing the periodogram.

### **University of Mumbai**

#### **Summer Examination 2022**

Program: ME Electronics Engineering Curriculum Scheme: Rev2016 Examination: ME Semester VIII

Course Code: ELXC 2022 and Course Name:Real Time System Design

Time: 2 hour 30 minutes Max. Marks: 80

Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	The Real Time systems are used
Option A:	primarily on mainframe computers
Option B:	for real-time interactive users
Option C:	for monitoring events as they occur
Option D:	for program development
	\$\delta \delta \
2.	The main components of an RFID passive tag include:
Option A:	Transceiver and Decoder
Option B:	Microchip and Antenna
Option C:	Antenna and Server
Option D:	None of the above
	\$\langle 2\cdot
3.	What is the maximum data rate of the RFID module?
Option A:	11 Mbps 25 25 25 25 25 25 25 25 25 25 25 25 25
Option B:	1 Kbps & Comment of the Comment of t
Option C:	10 Mbps 7 5 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6
Option D:	11 Gbps 7 7 7 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8
	470,49,43866660,600,496645
4.	In Cortex-M processor, NVIC stands for
Option A:	Nested Vectored Interrupt Controller
Option B:	Nested Voltage Interrupt Controller
Option C:	Nested Variable Interrupt Controller
Option D:	Nested Velocity Interrupt Controller
3000	1000 400 000 000 000 000 000 000 000 000
5.5.5	The main importance of ARM micro-processors is providing operation with
Option A:	Low cost and low power consumption
Option B:	Higher degree of multi-tasking
Option C:	Lower error or glitches
Option D:	Efficient memory management
6.7	Which of the following is correct in real time?
Option A:	non-preemptive kernels
Option B:	preemptive kernels
Option C:	neither preemptive nor non-preemptive kernels
Option D:	preemptive kernels or non-preemptive kernels
7,8899.4.	
00700	Semaphores are mostly used to implement
Option A:	system calls
Option B:	ipc mechanisms
Option C:	system protection

Option D:	System tasks
	\$\rightarrow\display \frac{\rightarrow}{\rightarrow} \ri
8.	What is the use of a content provider in Android?
Option A:	For sharing data between applications
Option B:	For storing data in the data base.
Option C:	For sending the data from an application to another
Option D:	For removing data from server
	\$\tau_1\tau_2\tau_
9.	Android is based on which Kernel?
Option A:	Linux
Option B:	Windows
Option C:	MAC
Option D:	Red hat
	\$27,89924 5,828 8,758 43.75 43.
10.	When program is loaded into the memory it is called as
Option A:	Procedure SEES SEES SEES SEES SEES SEES SEES SE
Option B:	Table STATE
Option C:	Register 5 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7
Option D:	Process 77777777777777777777777777777777777

Q2.	Solve any Two Questions out of Three 10 marks each	h
A	Explain Nested Vector Interrupt Controller and its features in ARM Corte M3 Processor.	:X-
В	Define and explain hard real time systems and soft real time systems wis suitable examples.	ith
С	Explain working principle of RFID. Elaborated on RFID components.	

Q3.	Solve any Two Questions out of Three	10 marks each
A	Explain the Memory Management Unit of ARM Cortex-M3	
B	Explain the structure of Android Applications.	
	Discuss OS security issues. Why is it important to implement	nt them?

Q4.	Solve any Two Questions out of Three	10 marks each
A A A A A A A A A A A A A A A A A A A	Explain in details steps involved in developing an er Railway Ticketing Database System.	nbedded system for
B	Explain the Context saving process and Retrieval process	in MicroOS/II.
	Explain the new strategies for assigning Real time tas systems.	sk to multiprocessor

## **University of Mumbai**

**Program: Electronics Engineering** 

Curriculum Scheme: Rev 2016 Examination: ME Semester II

Course Code: ELXC2021 and Course Name: Digital Design with Reconfigurable Architecture
Time: 2 hour 30 minutes

Max. Marks: 80

Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	In VHDL code the PORTS are described in
Option A:	Entity 7 9 8 8 8 8 9 9 9 7 9 9 8 8 8 9
Option B:	Architecture
Option C:	Library 2007 20 20 20 20 20 20 20 20 20 20 20 20 20
Option D:	Architecture and Library
	9 6 7 7 7 7 7 7 7 7 7 7 7 8 8 8 8 8 8 8 8
2.	In VHDL describes how the circuit should behave.
Option A:	Library SSTATES STATES AND
Option B:	Entity STATES ST
Option C:	Architecture
Option D:	Functions & San
3.	In Moore type FSM the output values are determined by its
Option A:	Clock input
Option B:	Current state
Option C:	Input values
Option D:	Next state A S S S S S S S S S S S S S S S S S S
57.7	- BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB
4.50	Process in VHDL is a statement
Option A:	Sequential
Option B:	Clock
Option C:	Delay
Option D:	Concurrent
25.7	Find the correct statement related to signal and variable in VHDL.
Option A:	Both signal and variable are global.
Option B:	Both signal and variable are local.
Option C:	Signal values are global whereas variable values are local.
Option D:	Signal values are local whereas variable values are global.
20000000000000000000000000000000000000	Find the correct statement related to IF, WAIT, CASE and LOOP used in VHDL.
Option A:	All IF, WAIT, CASE and LOOP are used for combinational code.
Option B:	All IF, WAIT, CASE and LOOP are used for sequential code.
Option C;	IF, WAIT are used for combinational code and CASE, LOOP are for sequential code.
Option D:	IF, WAIT are used for sequential code and CASE, LOOP are for combinational

	<u> </u>
	code.
	\$2000000000000000000000000000000000000
7.	Find correct statement related to constant in VHDL.
Option A:	Constant can be declared in Package only.
Option B:	Constant can be declared in Entity only.
Option C:	Constant can be declared in Architecture only.
Option D:	Constant can be declared in Package, Entity, Architecture.
	2,8,8,6,8,4,8,4,8,4,8,8,8
8.	Which of the following is not a type of modelling style?
Option A:	Behavioral modeling
Option B:	Dataflow modeling
Option C:	Structural modeling
Option D:	Component modelling
	\$
9.	Synchronous counters eliminate the delay problems encountered with
	asynchronous counters because
Option A:	input clock pulses are applied only to the first and last stages.
Option B:	input clock pulses are applied only to the last stage
Option C:	input clock pulses are not used to activate any of the counter stages
Option D:	input clock pulses are applied simultaneously to each stage
	242554552545444444
10.	A CPLD (Complex programmable logic device) is a collection of
Option A:	Multiple PLDs on a single integrated circuit
Option B:	Multiple ROM on a single integrated circuit
Option C:	Multiple RAM on a single integrated circuit
Option D:	Multiple flip flops on a single integrated circuit
	A. P. S A. W. A. A. A. A. A. S.

$\mathbf{Q2}$	Solve any Four out of Six (5 marks each)
SASS	Write differences between Moore machine and Mealy machine.
B	Draw only state diagram of Mealy machine to detect overlapping sequence 11001
	Write VHDL program for positive edge triggered D flip flop having active low reset pin.
A SEED SO	Describe all predefined operators used in VHDL.
STORE SO	Write a concurrent VHDL code for 8:1 Mux.
TO THE	Write short notes on," Block statements in VHDL code".

$\mathbf{Q3}$	Solve any Two Questions out of Three (10 marks each)
	Write VHDL code for ALU. The ALU should be capable of executing 8 arithmetic and 8 logical operations. Use 'when' statements for writing VHDL code.
B SSS	Write VHDL program for 5-stage shift register using signal assignment.
88999884999 999844509944 88489998449	Write a VHDL Code for sequence detector which produces an output Z=1 whenever input sequence 01101 occurs. Consider non overlapping sequence.

Q4	Solve any Two Questions out of Three (10 marks each)
A	Draw ASM chart for SHIFT and ADD multiplier and explain its working.
В	Design a 3 bit odd parity checker circuit for serial data. Use D flip flops.
С	Write short notes on:  (I) FPGA architecture  (II) CPLD Architecture