Question paper Sub_Mixed Signal VLSI Design_Rev-2016 (MCQ Section)

University Exam April-2021 ME
MCQ Section

Subject: Mixed Signal VLSI Design Course Code: ELXC1012
Semester: I
Year : April 2021 Branch: Electronics
Date: 24 / 04 / 2021 Time: 02:30 pm To 03:10 pm Marks : 40
College: Shah & Anchor Kutchhi Engineering College (126)

1] All questions are Compulsory
2] Assume suitable data wherever required.

* Required

1. Email address *

General Information

Fill it Carefully

2. Full Name of Student Beginning with surname *

3. Candidate Seat No. *

4. Candidate Mobile Number *

Q. Attempt all questions. [20*2=40M]

5. Condition for MOSFET in linear region ? *

Mark only one oval.

- Vds = Vgs
- Vgs = Vth
- Vds >= Vgs - Vth
- Vds <= Vgs - Vth

6. The voltage Vgs after which MOSFET will turn on ? *

Mark only one oval.

- Cutoff Voltage
- Threshold Voltage
- Pinch off Voltage
- Cut in Voltage

7. RAM circuit which is used in Main memory *

Mark only one oval.

- SRAM
- DRAM
- RAM
- ROM

8. Faster RAM circuit *

Mark only one oval.

- DRAM
- RAM
- ROM
- SRAM

9. EXPAND DLL *

Mark only one oval.

- Phase Locked Loop
- Dephase Locked Loop
- Delay Locked Loop
- Digital Locked Loop

10. An oscillator circuit which uses odd number of common source amplifiers *

Mark only one oval.

- Ring Oscillator
- Wien bridge Oscillator
- Crystal Oscillator
- Voltage controlled oscillator

11. _____ gate is used as a phase detector *

Mark only one oval.

- OR gate
- XOR gate
- AND gate
- NOR gate

12. PSA Stand for *

Mark only one oval.

- PMOS Sense Amplifier
- PMOS State Amplifier
- PMOS Select Amplifier
- PMOS Sense Angle

13. In a RAM array architecture column is calculated by *

Mark only one oval.

- Ccol = Colisub
- Ccol = (no. of word lines) X (cap of MOS S/D) + Ccolisub
- Ccol = Cap of MOS S/D
- Ccol = Rcol +Wcol

14. Problems associated with Sense Amplifier Design *

Mark only one oval.

- Kickback noise and Clock Circuit
- Kickback noise and Clock feed through
- Kickback noise and Carrier noise
- Clock feed through and operational noise

15. In ---------- circuit MOSFET is used as a switch *

Mark only one oval.

- Switched Capacitor
- Switched Resistor
- Switched Integrator
- Switched Amplifier

16. Noise created in sampling circuit *

Mark only one oval.

- White noise
- Jitter
- Thermal Noise
- Flicker Noise

17. Technique to reduce the effect of charge injection *

Mark only one oval.

- Add a dummy switch
- Add noise
- add JFET
- add BJT

18. Propagation delay is defined as *

Mark only one oval.

- tPHL =0.7(R1+R2)Cload
- tPHL =0.7(R1*R2)Cload
- tPHL =0.7(R1)Cload
- tPHL =0.7(R2)Cload

19. Coupling occurs due to parasitic capacitance between the ---------- lines *

Mark only one oval.

- Lower band
- Coupling
- Interconnect
- upper band

20. Power consumption is defined as *

Mark only one oval.

- Pavg = Vdd x Iavg
- Pavg = n Vdd
- Pavg = n Vdd x Iavg
- Pavg = n Iavg

21. 3 types of multivibrator circuits *

Mark only one oval.

- monostable, bistable, tristable
- monostable, quasistable, tristable
- monostable, distable, tristable
- monostable,bistable,stable

22. An electronic circuit that adds hysteresis to the input-output transition *

Mark only one oval.

- Sample and Hold circuit
- Switched Capacitor
- Schmitt Trigger
- Integrator

23. Mixed signal strategy consists of *

Mark only one oval.

- only interconnect level
- Interconnect level, device level, System level
- only device level
- only system level

24. ---------- are attached to the analog vdd supply for isolation *

Mark only one oval.

- plug
- switch
- rings
- Guard Ring

Question paper_ Mixed Signal VLSI Design_Rev-2016 (Descriptive Section)

University Exam ME April-2021
Descriptive Section

Subject: Mixed Signal VLSI Design Course Code: ELXC1012
Semester: I
Year : April 2021 Branch: Electronics
Date: 24 / 04 / 2021 Time: 3.10 pm To 04.30 pm Marks : 40
College: Shah & Anchor Kutchhi Engineering College (126)

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4. Candidate's mobile number

Attempt all questions. [40M]

Write answers on plane paper(A4 size), scan and upload the PDF for Q2 separately and Q3 separately.
Please write Year, Semester, Branch and seat no. on every page
Assign page number to each page(e.g. page 1 of 5, page 2 of 5 and so on)
Sign on each page.

5. Q.2 Solve any two out of three 10 marks each A] Draw and Explain ROM array using NOR-NOR logic? B] Explain charge pump PLL with neat diagram and output graph. C] Explain Ring oscillator circuit with neat diagram? *

   Files submitted:

6. Q3 Solve any two out of three 10 marks each A] Explain the concept of flash ADC with neat diagram? B] Explain sense amplifier final design circuit with circuit diagram? C] Explain non ideal effects of PLL circuit? *

   Files submitted: