Question paper(MCQ Section) Sub: APA II Sem:ME SEM II Scheme: R2016 Branch:Electronics

University Exam August-2021
MCQ Section

Session: August-2021
Scheme: R2016
Branch: Electronics
Subject: APA II
Subject Code: ELXDLO2021
Year: ME
Semester: II
Date: 12-08-2021
Time: 11.30 AM to 12.10 PM
Maximum Marks: 40

1] All questions are Compulsory
2] Assume suitable data wherever required.

The respondent's email (**null**) was recorded on submission of this form.
* Required

1. Email *

General Information

Fill it Carefully

2. Full Name of Student Beginning with surname *

3. Candidate Seat No. *

4. Candidate Mobile Number *

Q. Attempt all questions. [20*2=40M]

5. Way in which the components are interrelated is known as, *

Mark only one oval.

- function
- structure
- states
- tasks

6. MAR refers as, *

Mark only one oval.

- Memory data Register
- Memory Register
- Memory counter
- Memory Address Register

7. MIPS rate of a processor is given by *

Mark only one oval.

- f / T
- f / 10^6
- f / CPI
- f / CPI x 10^6

8. In main memory structure ---------- number of blocks are present with n bit address and k words *

Mark only one oval.

- 2^n
- 2^n / k
- k
- k/n

9. Cache memory is divided into number of---------- *

Mark only one oval.

- blocks
- lines
- words
- units

10. List the order of computer function *

Mark only one oval.

- data processing, data storage, control, data movement
- data processing, data storage, data movement, control
- data storage, data processing, data movement, control
- data processing, data movement, control, data storage

11. Computer top level structure consists of, *

Mark only one oval.

- CPU, Memory, I/O, Interconnection
- I/O, CPU, Interconnection, Memory
- CPU, I/O, Memory, Interconnection
- Memory, I/O, Interconnection,CPU

12. The processor time T needed to execute a given program is expressed as, *

Mark only one oval.

- T = Ic x CPI
- T = Ic x z
- T = Ic x CPI x z
- T = Ic /CPI x z

13. In a direct mapped cache memory organization, number of blocks in main memory, *

Mark only one oval.

- 2^n
- 2 x s
- 2 x n
- 2^s

14. Size of tag in a direct mapped cache organization is, *

Mark only one oval.

- s bits
- r bits
- (s-r) bits
- r-s bits

15. If a program happens to refer words repeatedly from two different blocks that map into the same line it is called, *

Mark only one oval.

- blocking
- thrashing
- transfer
- processing

16. In associative mapping how main memory address is divided *

Mark only one oval.

- Tag + Word
- Tag
- Word
- Tag + line + word

17. Size of cache in k way set associative cache organization is, *

Mark only one oval.

- K words
- 2 ^d words
- k x 2^d+w words
- 2 ^ d+w words

18. RAID has how many levels? *

Mark only one oval.

- 4
- 5
- 6
- 7

19. Pentium 4 has how many caches? *

Mark only one oval.

- L1
- L1, L2
- L2
- L1, L2, L3

20. ---------- Algorithm is used in PCI arbitration? *

Mark only one oval.

- Least recently used algorithm
- Fairness Algorithm
- First in First out
- Last in First out

21. PCI has transfer rate of? *

Mark only one oval.

- 130 Mbytes/sec
- 135 Mbytes/sec
- 132 Mbytes/sec
- 140 Mbytes/sec

22. ----------is the interface control signal of PCI bus? *

Mark only one oval.

- FRAME #
- GNT #
- CLK
- PAR 64

23. Arbitration of PCI bus happens with, *

Mark only one oval.

- REQ #
- GNT #
- LOCK #
- REQ # and GNT # signals

24. Redundancy through hamming code is maintained in *

Mark only one oval.

- RAID 1
- RAID 2
- RAID 3
- RAID 4

Question paper(Descriptive Section) Sub: APA II Sem: ME SEM II Scheme: R 2016 Branch:Electronics

University Exam June-2021
Descriptive Section

Session: August-2021
Scheme: R2016
Branch: Electronics
Subject: APA II
Subject Code: ELXDLO2021
Year: ME
Semester: II
Date: 12 -08-2021
Time: 12.10 PM to 1.30 PM
Maximum Marks: 40
1] All questions are Compulsory
2] Assume suitable data wherever required.

* Required

1. Email *

General Information

Fill it Carefully

2. Full Name of Student Beginning with surname *

3. Candidate Seat No. *

4. Candidate's mobile number

Attempt all questions. [40M]

Write answers on plane paper(A4 size), scan and upload the PDF for Q2 separately and Q3 separately.
Please write Year, Semester, Branch and seat no. on every page
Assign page number to each page(e.g. page 1 of 5, page 2 of 5 and so on)
Sign on each page.
Both Q2 and Q3 are compulsory
Any 2 sub questions each of Q2 and Q3 are to be attempted..

5. Q2) a) Draw timing diagram of PCI write transfer and explain the same?[10 marks] b) Explain main features, objectives and functions of operating system? [10 marks] c) What is USB? Explain the different types of transfers in USB? [10 marks] *

   Files submitted:

6. Q3) a) Explain RAID and it's types with neat diagram? [10 marks] b) Explain how cache coherency is maintained in multiprocessor implementation? [10 marks] c) Explain the features of VLIW? Explain pitfalls in VLIW architecture? [10 marks] *

   Files submitted:

ELXC 2023 Advanced signal Processing_Rev-2016 (MCQ Section)

ESE August 2021
MCQ Section

Subject: Advanced Signal Processing Course Code:ELXC 2023
Semester: 2
Year : 2021 Branch: Electronics
Date: 10/ 08 / 2021 Time: 11:30 pm To 12:10 pm Marks : 40
College: Shah & Anchor Kutchhi Engineering College (126)

1] All questions are Compulsory
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The respondent's email (**null**) was recorded on submission of this form.
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General Information

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2. Full Name of Student *

3. Candidate Seat No. *

4. Candidate Mobile Number *

Q. Attempt all questions. [20*2=40M]

5. _____ function is an even function *

Mark only one oval.

- Power spectrum density
- Linear convolution
- Auto correlation
- Cross correlation

6. The mean value of a wide sense stationary process is _____ *

Mark only one oval.

- Variable
- Constant
- Zero
- Can not be determined

7. Fourier tranform does not exist for a stationary random process.This statement is _____ *

Mark only one oval.

- True
- False
- Sometimes true
- Sometimes false

8. The spectral characteristics of a random process is obtained by computing the _____of the autocorrelation function *

Mark only one oval.

- ◯ Z transform
- ◯ Fourier transform
- ◯ Laplace transform
- ◯ Discrete cosine transform

9. In an ergodic process the time average obtained from a single realization is _____the statistical average *

Mark only one oval.

- ◯ greater than
- ◯ less than
- ◯ equal to
- ◯ double that of

10. An all pole filter function corresponds to _____process *

Mark only one oval.

- ◯ AR
- ◯ MA
- ◯ ARMA
- ◯ MARA

11. _____ is the Fourier transform of the autocorrelation function *

Mark only one oval.

- Power spectrum density
- Energy spectrum density
- Cross power spectrum density
- square of the PSD

12. Periodogram is not a consistent estimate of the true power density.This statement is _____ *

Mark only one oval.

- False
- True
- Not always false
- Not aiways true

13. An all zero filter function corresponds to _____process *

Mark only one oval.

- AR
- MA
- ARMA
- MARA

14. Which of the PSD estimation methods provide better frequency resolution? *

Mark only one oval.

- Conventional
- Non conventional
- Parametric
- Nonparametric

15. In decimation and interpolation processes _____filter is used *

Mark only one oval.

- Highpass
- Lowpass
- Bandpass
- Bandstop

16. Multifold periodic repetition of the input signal spectrum is generated in _____ *

Mark only one oval.

- Decimation
- Convolution
- Correlation
- Interpolation

17. Which of the following methods suffer from spectral leakage effects? *

Mark only one oval.

- Conventional
- Nonconventional
- Parametric
- Nonparametric

18. A system function which has both finite poles and zeros in the z plane corresponds to _____process *

Mark only one oval.

- MARA
- AR
- MA
- ARMA

19. In decimation process by a factor D ,the cutoff frequency of the filter is *

Mark only one oval.

- pi/(3D)
- pi/D
- pi/(2D)
- pi/(4D)

20. QRS complex analysis is done in _____signal processing *

Mark only one oval.

- Radar
- Sonar
- Seismic
- Biomedical

21. When interpolation is done by a factor I _____ zeros are inserted between sccessive values of x(n) *

Mark only one oval.

- I
- 2I
- I-1
- 2(I-1)

22. Sampling rate conversion by a rational factor can be achieved by cascading _____ left to right *

Mark only one oval.

- a decimator with an interpolator
- a decimator with another decimator
- an interpolator with a decimator
- an interpolator with another interpolator

23. In which of the following applications significant frequency components lie in the range of 4 to 45Hz *

Mark only one oval.

- Seismic signal Processing
- Speech processing
- Sonar signal processing
- QRS complex analysis

24. Cross correlation function can be most suitably used for measuring _____ *

Mark only one oval.

- Similarity between 2 signals
- Dissimilarity between signals
- output of the system
- energy of a signal

ELXC 2023 Advanced signal Processing_Rev-2016 (Descriptive Section)

ESE August 2021
Descriptive Section

Subject: Advanced Signal Processing Course Code:ELXC 2023
Semester: 2
Year : 2021 Branch: Electronics
Date: 10/ 08 / 2021 Time: 12:10 pm To 1:30 pm Marks : 40
College: Shah & Anchor Kutchhi Engineering College (126)

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2. Full Name of Student *

3. Candidate Seat No. *

4. Candidate's mobile number *

Attempt all questions. [40M]

Write answers on plane paper(A4 size), scan and upload the PDF for Q2 separately and Q3 separately.
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Assign page number to each page(e.g. page 1 of 5, page 2 of 5 and so on)
Sign on each page.
Both Q2 and Q3 are compulsory
Any 2 sub questions each of Q2 and Q3 are to be attempted..

5. Q2 *

Q2) a) Derive the equations for the spectrum of a signal which is interpolated by a factor I. Draw the spectral diagrams. (10 Marks)

b) Describe any one non parametric method of PSD estimation. (10 Marks)

c) Explain biomedical applications of DSP. (10 Marks)

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6. Q3 *

Q3) a) Explain decimation in multirate signal processing with equations and spectral diagrams. (10 Marks)

b) Give the details of Bartlett method of averaging periodogram with equations. (10 Marks)

c) How Wiener filter can be modified as a linear predictor ? Also explain how adaptive noise cancellation can be achieved? . (10 Marks)

Files submitted:

Digital Design with Reconfigurable Architecture MCQ

University Exam August 2021

Subject: Digital Design with Reconfigurable Architecture
Course Code: ELXC2021 Semester: II
Year : ME Branch: ETRX
Date: 05 / 08 / 2021 Time: 11.30am To 01.30 pm Marks :40
College: Shah & Anchor Kutchhi Engineering College (126)

1] All questions are Compulsory

The respondent's email (**null**) was recorded on submission of this form.
* Required

1. Email *

2. Full Name of the student *

3. Candidate Seat number *

4. Candidate Mobile Number *

Attempt all questions. [40M]

Each Question carry two marks

5. It describes the behavior of electronic circuit or systems, from which the physical circuit or system can be implemented *

Mark only one oval.

- Scripting Programming Language
- Procedural Programming Language
- Hardware Description Language
- Object Oriented Language

6. What is the basic unit of structural modeling? *

Mark only one oval.

- Process
- Component instantiation
- Component declaration
- Block

7. Which mechanism allocates the binary value to the states in order to reduce the cost of the combinational circuits? *

Mark only one oval.

- State Reduction
- State Minimization
- State Assignment
- State Evaluation

8. Sequential operations in digital system are described by *

Mark only one oval.

- MAP
- Flow Chart
- ASM Chart
- Graph

9. Bottle dispenser can be implemented is VHDL using *

Mark only one oval.

- Vending Machine design logic
- Sequential circuit design logic
- Microprocessor logic
- Combinational design logic

10. In this modeling style, the flow of data through the entity is expressed using concurrent (parallel) signal. Like WHEN and GENERATE. *

Mark only one oval.

- Data Flow Modelling
- Behavioral Modelling
- Structural Modelling
- Object oriented Modeling

11. What is function of below VHDL code? *

```
VHDL Code:

Library ieee;
use ieee.std_logic_1164.all;

entity sample is
   port(a,b:in bit ; c:out bit);
end xnor1;

architecture behavioural of xnor1 is
begin
   c<=not(a xor b);
end behavioural;
```

Mark only one oval.

- ( ) NOR GATE
- ( ) OR-GATE
- ( ) X-NOR GATE
- ( ) X-OR GATE

12. In below VHDL code TYPE state specifies *

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
---------------------------------------------------
ENTITY <entity_name> IS
   PORT ( input: IN <data_type>;
          reset, clock: IN STD_LOGIC;
          output: OUT <data_type>);
END <entity_name>;
---------------------------------------------------
ARCHITECTURE <arch_name> OF <entity_name> IS
   TYPE state IS (state0, state1, state2, state3, ...);
   SIGNAL pr_state, nx_state: state;
BEGIN
   ---------- Lower section: -----------------------
   PROCESS (reset, clock)
   BEGIN
      IF (reset='1') THEN
         pr_state <= state0;
      ELSIF (clock'EVENT AND clock='1') THEN
         pr_state <= nx_state;
      END IF;
   END PROCESS;
   ---------- Upper section: -----------------------
   PROCESS (input, pr_state)
   BEGIN
      CASE pr_state IS
         WHEN state0 =>
            IF (input = ...) THEN
               output <= <value>;
               nx_state <= state1;
            ELSE ...
            END IF;
         WHEN state1 =>
            IF (input = ...) THEN
               output <= <value>;
               nx_state <= state2;
            ELSE ...
            END IF;
```

Mark only one oval.

- ( ) Variable
- ( ) Enumerated data type
- ( ) Signal
- ( ) Component

13. The concurrent assignment statement is activated whenever _____ *

Mark only one oval.

- ( ) The execution is scheduled
- ( ) The waveform associated changes its value
- ( ) The process is terminated
- ( ) The value of the target is needed

14. A user wants a constant to be declared in such a way that it can be accessible by whole code, where should the user declare this constant? *

Mark only one oval.

- Architecture
- Configuration
- Package
- Entity

15. For programmable logic functions, which type of PLD should be used? *

Mark only one oval.

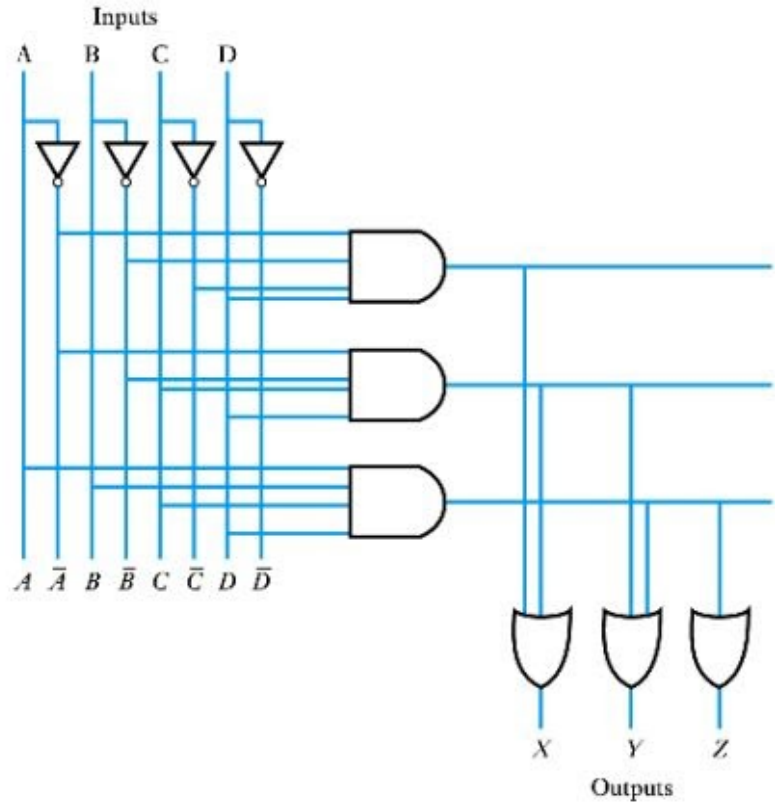
- PLA
- PAL
- CPLD
- SLD

16. Which type of device FPGA are? *

Mark only one oval.

- SLD
- SROM
- EPROM
- PLD

17. In the following PLA, which output implements the logic function ABCD? *



Mark only one oval.

- X
- Y
- Z
- X AND Z

18. RTL stands for *

Mark only one oval.

- Register-Transfer Level
- Register Timing Level
- Register Timing Language
- Register Transfer Loop

19. Which of the following statement is not an advantage of Programmable Logic Devices (PLD's) *

Mark only one oval.

- Short Design Cycle
- Increased Space requirement
- Increased Flexibility
- Reprogrammable

20. For using a process to implement a combinational circuit, which signals should be in the sensitivity list? *

Mark only one oval.

- Inputs of the circuit
- Outputs of the circuit
- Both of the Inputs and Outputs
- No signal should be in the sensitivity list

21. ---------- describes the input / output port. *

Mark only one oval.

- An Entity
- An Architecture
- Signal
- Variable

22. Most FPGA logic modules utilize a ----------approach to create the desired logic functions *

Mark only one oval.

- Look-up Table
- Only AND array
- AND-OR Array
- Memory Element

23. Below VHDL code will be executed in ---------- *

```
library ieee;
use ieee.std_logic_1164.all;

entity enc is
   port(i0,i1,i2,i3,i4,i5,i6,i7:in bit; o0,o1,o2: out bit);
end enc;

architecture vci of enc is
begin
   o0<=i4 or i5 or i6 or i7;
   o1<=i2 or i3 or i6 or i7;
   o2<=i1 or i3 or i5 or i7;
end vci;
```

Mark only one oval.

- Sequentially
- Concurrently
- Both sequential as well as concurrent
- Will give error

24. This is graphical method of identifying redundant states *

Mark only one oval.

- Implication Chart Method
- Partition minimization method
- Inspection Method
- State Assignment Method

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AY 2020-21 ME

AY 2020-21 ME Students

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Google Meet Link

https://meet.google.com/xms-yhwc-gst

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2) Attendance link will be posted in the Google Classroom at 11.30 AM
3) Students should fill the attendance form properly.

4) At scheduled time link for the Question Paper will be posted in the classroom.
5) The exam will be for two hours.
6) Submit MCQ at 12.10 pm sharp
7) Subjective link will be posted at 12.10pm
8) Write Q.2, Q.3 in white plain paper with black ink and upload each individually
9) For any queries contact me at 9004048302

Add class comment...

Babychen Mathew ▸ 1 student
Jul 29

https://forms.gle/oNRUtbnayNSzDpCS9

ASP VIVA attendance link

Add class comment...

Annexure B

University of Mumbai

Examination summer 2021 under cluster_____(Lead College: SAKEC)

Examinations Commencing from 5th August 2021

Program:

All

Curriculum Scheme: **Rev2016**

Examination: **ME Semester II**

Course Code: **ELXC2022** and

Course Name: **Real Time System Design**

Time: 2-hour Max. Marks: 80

==========

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	---------- are mainly used in toll booth payments and security access control systems whereas -------- are very common in mining, oil and gas and cargo tracking industrial applications.
Option A:	Active tags, Passive tags
Option B:	Low frequency, High Frequency
Option C:	Transponder tags, Beacon tags
Option D:	small size, large size
2.	In an embedded system reducing clock frequency results to …
Option A:	Increase in power consumption
Option B:	decrease in power consumption
Option C:	Increase in performance
Option D:	Decrease in execution time
3.	Which of the following is an example of 2 wire Communication Interface?
Option A:	I2C
Option B:	Wi-Fi
Option C:	Ethernet
Option D:	IEEE1394
4.	In a CAN bus ----------protocol is implemented.
Option A:	TDMA
Option B:	CDMA CA
Option C:	CSMA CD
Option D:	FDMA
5.	-------- is noise that can be mistaken by a authorized RFID signal which is a serious issue in -------- and security systems
Option A:	eavesdropping, trolling
Option B:	Ghost Read, inventory
Option C:	Interception, transport

Option D:	eavesdropping, transport
6.	Specify the type of motor used for alignment and throttle control in Adaptive Cruise Control.
Option A:	DC motor
Option B:	AC motor
Option C:	Stepper motor
Option D:	Servo Motor
7.	Interrupt priority is needed to ----------
Option A:	Interrupt the processor unnecessarily
Option B:	To resolve priority conflicts due to concurrent arriving interrupts
Option C:	To disable nesting of interrupts
Option D:	To reduce interrupt latency
8.	RS-485 supports maximum cable length of _____and Data rate up to -----
Option A:	4000ft, 100KB/S
Option B:	3000ft, 100KB/S
Option C:	4000ft, 200KB/S
Option D:	3000ft, 200KB/S
9.	Flexibility is the ability to change the ------ of the system without incurring heavy ---- cost.
Option A:	operation, unit
Option B:	functionality, NRE
Option C:	design, manufacturing
Option D:	execution, maintenance
10.	What is the primary objective of White box testing?
Option A:	To check the efficiency of an application
Option B:	To check the I/O interface of an application
Option C:	To check internal structure and working of an application
Option D:	To check the failure rate of an application
11.	---------- is used for exchanging data between multiple threads in one or more processes or programs.
Option A:	POSIX
Option B:	IPC
Option C:	ISR
Option D:	#INCLUDE
12.	In a robot a task that gets generated to handle an obstacle that suddenly appears is a ----------
Option A:	Periodic
Option B:	Aperiodic
Option C:	Running
Option D:	Sporadic
13.	The necessary Test of schedulability states that total CPU Utilization to

	be --------
Option A:	=square(n)
Option B:	=n*((2^(1/n)) - 1)
Option C:	0.8242
Option D:	0.7767
14.	Which is the function call used by an ISR to indicate the occurrence of an interrupt to the Micro-C/OS-II kernel
Option A:	Interrupt
Option B:	OSIntEnter
Option C:	OSIntExit
Option D:	OSIntNesting
15.	The ---------- must be less than a defined value for a specific task execution in real time systems.
Option A:	Memory
Option B:	Latency
Option C:	Bandwidth
Option D:	Cost
16.	----------helps maintain portability and compatibility between different operating systems.
Option A:	POSIX
Option B:	IPC
Option C:	ISR
Option D:	RPC

17.	Micro-C OS/II function ---------- delays the task for the specified duration.
Option A:	OSTimeDlyHMSM ()
Option B:	OSTimeDlyResume ()
Option C:	OSTimeSet ()
Option D:	OSTimeGet ()
18.	---------- is also called interrupt level; -------- is called task level.
Option A:	Foreground, background
Option B:	background, Foreground
Option C:	kernel, RTOS
Option D:	Latency, synchronization
19.	The Cortex-M3 contains two stack pointers (R13) which are ….
Option A:	PRIMASK, FAULTMASK
Option B:	Main Stack Pointer and Process Stack Pointer
Option C:	The Link Register and The Program Counter
Option D:	Control register and BASEPRI
20.	In the Cortex-M3 --------- stops the processor clock and ---------- stops the system clock and switches off the PLL and flash memory.

Option A:	Sleep-on-exit, Sleep-on-entry
Option B:	WFE mode, SEV mode
Option C:	sleep mode, deep sleep mode
Option D:	The SYSTICK Timer mode and Power Management mode

Q2. (20 Marks)	**Solve any Two Questions out of Three 10 marks each**
1	Discuss the built-in Nested Vectored Interrupt Controller of Cortex - M3.
2	What protocols are used to communicate between RFID reader and tag. Explain RFID middleware architecture.
3	List and explain task related functions calls in uC/OS-III.

Q3. (20 Marks)	**Solve any Two Questions out of Three 10 marks each**
1	With neat diagram explain the structure of Android application.
2	Design an embedded system for elevator control by discussing following issues: a) Requirement Analysis b) Program model c) Hardware and software architecture d) Testing and debugging with real time issues.
3	Discuss the points to be considered while choosing an RTOS.

Program: **Comp, IT, ETRX**
Curriculum Scheme: Rev2016
Examination: ME Semester II (2021)
Course Code: IL02027 and Course Name: IPR and Patenting
Time: 2 hour Max. Marks: 80
==========

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	_____ is such a property not occurring in nature but an intangible creation of the human mind
Option A:	Intellectual property
Option B:	Assets
Option C:	Cash
Option D:	Money
2.	Copyright Act was introduced in India in
Option A:	1947
Option B:	2020
Option C:	2021
Option D:	1957
3.	A trademark is represented by several key characteristics. Which of the following is one of them?
Option A:	Slogans are not covered under trademark law
Option B:	A trademark identifies a product's origin
Option C:	Trademarks are "shorthand" for retailers to use in determining pricing strategy
Option D:	Trademarks are never an indicator of quality
4.	Certain IP rights are time bound and called as
Option A:	limited period IP
Option B:	lapsable IP right
Option C:	limited life IP right
Option D:	time bound IPR
5.	The headquarters of the Design wing in India is situated at -
Option A:	Kolkata
Option B:	Goa
Option C:	Mumbai
Option D:	Delhi
6.	Indirect infringement is a kind of ..... infringement.

Option A:	secondary
Option B:	primary
Option C:	punishable
Option D:	shared
7.	TRIPS stand for
Option A:	Trade Related Aspects of Intellectual Personal Rights
Option B:	Trade Related Aspects of Intellectual Property Rights
Option C:	Trade Relation Aspects of International Property Rights
Option D:	Trade Relations Attributes of Intellectual Property Rights
8.	_____ is an essential part of E-Commerce business, as branding, customer recognition and good will.
Option A:	Watermark
Option B:	Trademark
Option C:	Logo
Option D:	Photos
9.	IP consists of new ideas, original expressions, distinctive names, and appearance that make products
Option A:	Famous
Option B:	Similar as others
Option C:	unique and valuable
Option D:	Easy To sell in E commerce
10.	Which of the following is one of the IP challenges in a digital economy?
Option A:	Access
Option B:	Difficulties with finding the infringer
Option C:	Watermark
Option D:	Photos
11.	Patent application can be filed in India by
Option A:	True and First Inventor only
Option B:	Assignee of the inventor only
Option C:	Legal representative of the inventor only
Option D:	Inventor/assignee/legal representative
12.	Kinds of specifications involved in patent drafting are
Option A:	Non provisional specification
Option B:	Complete specifications only

Option C:	Provisional specification only
Option D:	Provisional and Complete Specification
13.	Patent of addition can be filed by
Option A:	Only Inventor
Option B:	Only patentee
Option C:	Inventor as well as patentee
Option D:	patent agent
14.	A grant of a European patent may be requested for how many states
Option A:	one or more of the Contracting States
Option B:	One
Option C:	Two
Option D:	three
15.	What is USPTO?
Option A:	United States Patent and Trade Office
Option B:	United States Panel and Trademark Office
Option C:	United States Patent and Trademark Office
Option D:	United States Patent and Transaction Office
16.	Which one is not an intangible asset?
Option A:	Inventory
Option B:	Brandname
Option C:	Databases
Option D:	Goodwill
17.	..... means a feature of an invention that involves technical advance as compared to the existing knowledge or having economic significance or both and that makes the invention not obvious to a person skilled in the art;
Option A:	patent of addition
Option B:	Patent
Option C:	inventive step
Option D:	new invention
18.	You can infringe a patent by:
Option A:	Making a product for your own personal use
Option B:	Making different products to the invention in order to research their technical effectiveness
Option C:	Selling the main components of the product, together with instructions how to assemble it using commonly available fastening components such as nuts, bolts, cable-ties and so on
Option D:	Publishing drawings of the product on your website
19.	Prior art search includes

Option A:	Search of Patent literatures only
Option B:	Search of Non-patent literature only
Option C:	Search of patent ideas only
Option D:	Search of patent as well as Non-patent literature
20.	An exclusive license confers rights
Option A:	To the exclusion of all other persons including the Patentee
Option B:	To the exclusion of all other persons excluding the Patentee
Option C:	Exclusively to the Patentee
Option D:	To the assignee

Q2.	**Solve any Four out of Six** **5 marks each**
A	Describe the rights covered under intellectual property rights.
B	What is the importance of IP Rights?
C	Enumerate the key concerns of counterfeiting / piracy.
D	List and explain the international treaties and conventions on Intellectual Property.
E	What are the challenges to Intellectual Property in ecommerce?
F	Explain in brief about Intellectual Property and Bio-diversity.

Q3.	**Solve any Four out of Six** **5 marks each**
A	Explain the contents of the patent application.
B	Discuss the major steps involved to get a patent.
C	Write a short note on Patent Search Databases.
D	Write a short note on the International Scenario of Patent Rules.
E	List and explain types of patent applications.
F	Identify the conditions of patentability.