Examination 2021 under Cluster 06

(Lead College: Vidyavardhini's College of Engg Tech)

Examinations Commencing from June 01, 2021

Program: **Electronics Engineering**Curriculum Scheme: Rev 2016

Examination: TE Semester VI

Course Code: ELX601 and Course Name: Embedded Systems and Real Time Operating System

Time: 2 hour Max. Marks: 80

| Q1. | Choose the correct option for following questions. All the Questions are compulsory and carry equal marks |
|-----------|---|
| | |
| 1. | circuit prevents the processor/controller from unexpected program |
| | execution behavior when the supply voltage to the processor/controller falls |
| Option A: | below a specified voltage. Reset |
| Option B: | Brown out protection |
| Option C: | Watchdog |
| Option C: | Programmable Peripheral Interface |
| Орион В. | 1 Togrammable 1 empherar interface |
| 2. | Ais a computer program that operates or controls a particular type of |
| | device that is attached to a computer. |
| Option A: | device disk |
| Option B: | ISR |
| Option C: | device driver |
| Option D: | IPC |
| • | |
| 3. | In Black Box Testing, the tester |
| Option A: | is not knowing the internal architecture or structure/techniques of the functional |
| _ | block to be tested. |
| Option B: | is fully aware the internal architecture or structure/techniques of the functional |
| | block to be tested. |
| Option C: | is independent and has no idea of data, requirements or specifications. |
| Option D: | is not required. |
| | |
| 4. | The smart card reader communicates with a desktop machine by implementing a |
| | communication channel using |
| Option A: | RS-232 C |
| Option B: | ZigBee |
| Option C: | GPRS |
| Option D: | RS-485 |
| | |
| 5. | The most important phase in software life cycle is |
| Option A: | Integration |
| Option B: | Design |

| Option C: | Testing |
|-----------|---|
| Option D: | Debugging |
| opnon 2. | |
| 6. | is a timing device that resets the system after a predefined timeout |
| Option A: | Real time clock |
| Option B: | Reset circuit |
| Option C: | Watchdog timer |
| Option D: | Power down mode |
| | |
| 7. | is fast in operation due to its resistive networking and switching |
| | capabilities |
| Option A: | NVRAM |
| Option B: | DRAM |
| Option C: | SRAM |
| Option D: | RAM |
| | |
| 8. | is a term used to describe a situation when a higher priority task cannot |
| | execute because it is waiting for a low priority task to complete. |
| Option A: | IPC |
| Option B: | Priority Inheritance Protocol |
| Option C: | Priority Inversion |
| Option D: | Priority Ceiling |
| 9. | The two common kinds of semaphores are |
| Option A: | Binary and Counting |
| Option B: | Primary and Secondary |
| Option C: | Signal and Pipe |
| Option D: | Single and Mailbox |
| 10. | is used to acquire semaphore in uCOS-II. |
| Option A: | OSSemPost() |
| Option B: | OSSemphore () |
| Option C: | OSSemAcq () |
| Option D: | OSSemPend() |
| 11. | The fundamental building blocks of UML are |
| | |
| Option A: | Structure and behaviour |
| Option B: | Things, relationships and diagrams |
| Option C: | Objects and classes |
| Option D: | Use case and sequence diagrams |
| | |
| 12. | Which of the following is one-time programmable memory? |
| Option A: | SRAM |
| Option B: | PROM |
| Option C: | FLASH |
| Option D: | NVRAM |

| 13. | Which of the following are the three measures of information security in |
|-----------|--|
| 13. | embedded systems? |
| Option A: | Confidentiality, secrecy, integrity |
| Option B: | Confidentiality, integrity, availability |
| Option C: | Confidentiality, transparency, availability |
| Option C: | Integrity, transparency, availability |
| Option D. | integrity, transparency, availability |
| 14. | A situation where none of the processes are able to make any progress in their execution is termed as |
| Option A: | Deadlock |
| Option B: | Livelock |
| Option C: | Starvation |
| Option D: | Racing |
| | |
| 15. | The state where a process is incepted into the memory and awaiting the processor time for execution is known as |
| Option A: | Ready State |
| Option B: | Blocked State |
| Option C: | Waiting State |
| Option D: | Created State |
| • | |
| 16. | The ability of an operating system to hold multiple process in memory and switch the processor (CPU) from executing one process to another process is called |
| Option A: | Multitasking |
| Option B: | Multiprocessing |
| Option C: | Multiprogramming |
| Option D: | Multithreading |
| | |
| 17. | is a sleep and wakeup based mutual exclusion implementation for shared resource access |
| Option A: | Mutex |
| Option B: | Remote Procedure call |
| Option C: | Semaphore |
| Option D: | Racing |
| | |
| 18. | Which is the function call used by an ISR to indicate the occurrence of an interrupt to the MicroC/OS-II Kernel |
| Option A: | Interrupt |
| Option B: | OSIntEnter |
| Option C: | OSIntExit |
| Option D: | OSIdle |
| | |
| 19. | RS 232 is not suitable for communications. |
| Option A: | Point to Point |
| Option B: | Multi Drop |
| Option C: | 2 Wire communication |
| Option D: | Mesh network |
| 1 | |
| | , |

| 20. | is not a task type. |
|-----------|---------------------|
| | |
| Option A: | Periodic |
| Option B: | Sporadic |
| Option C: | Priority Inversion |
| Option D: | Aperiodic |

| 2 | Solve any Two Questions out of Three | 10 marks each |
|------------|--|-------------------|
| (20 Marks) | | |
| A | What is the role of sensor and transducer in Embedded Illustrate with an example. | 1 System design? |
| В | Explain the different types of UML diagram and their sig stage of the system development life cycle. | mificance in each |
| С | Explain Rate Monotic Scheduling Algorithm; State its disadvantages. | advantages and |

| Q Q3. (20 Marks) | Solve any Two Questions out of Three 10 marks each |
|------------------|--|
| A | Design a Car Cruise-control using uCOS II RTOS. Support the design with |
| В | requirements, hardware and software architecture. Write a short not on: Hardware-Software Co-design |
| С | What are the different types of Inter-process communication? Explain any two in detail. |

Examination 2021 under Cluster 06

(Lead College: Vidyavardhini's College of Engg Tech)

Examinations Commencing from June 01, 2021
Program: Electronics Engineering

Curriculum Scheme: Rev 2016 Examination: TE Semester VI

Course Code:ELX602 and Course Name: Computer Communication and Networks Time: 2 hour Max. Marks: 80

| Q1. | Choose the correct option for following questions. All the Questions are compulsory and carry equal marks |
|-----------|--|
| | |
| 1. | We add r redundant bits to each block to make the length $n = k + r$. The resulting n-bit blocks are called |
| Option A: | Blockword |
| Option B: | Dataword |
| Option C: | Code word |
| Option D: | Word |
| • | |
| 2. | Which error detection method uses one's complement arithmetic? |
| Option A: | Simple parity check |
| Option B: | CRC |
| Option C: | Two-dimensional parity check |
| Option D: | Checksum |
| | |
| 3. | Automatic repeat request error management mechanism is provided by |
| Option A: | logical link control sublayer |
| Option B: | media access control sublayer |
| Option C: | network interface control sublayer |
| Option D: | application access control sublayer |
| | |
| 4 | In PURE ALOHA, vulnerable time isframe transmission time. |
| Option A: | the same as |
| Option B: | two times |
| Option C: | three times |
| Option D: | four times |
| | |
| 5. | Devices in a ring or mesh topology are usually configured in arelationship |
| Option A: | Peer to peer |
| Option B: | Point to Point |
| Option C: | primary to secondary |
| Option D: | Master & slave |
| 1 | |
| 6. | In a mesh topology with n devices, if a new device is added,new links are needed. |
| Option A: | n |

| Option B: | n-1 |
|-----------|--|
| Option C: | n+1 n+1 |
| Option C: | 2n |
| Орион Б. | Zii |
| 7. | A device that helps prevent congestion and data collisions is |
| Option A: | Switch |
| Option B: | Hub |
| Option C: | Gateway |
| Option D: | Proxy Server |
| 8. | In the Ethernet frame, the field contains error detection information. |
| Option A: | Address |
| Option B: | Preamble |
| Option C: | CRC |
| Option D: | Type |
| | |
| 9. | In the Ethernet, thefield is actually added at the physical layer and is not (formally) the part of the frame. |
| Option A: | address |
| Option B: | CRC |
| Option C: | Preamble |
| Option D: | Type of protocol |
| 10. | The MAC (Media Access Control) address of the network card is used in both Ethernet and Token-Ring networks and is essential for communication. What does MAC provide? |
| Option A: | An alias for the computer name. |
| Option B: | The logical domain address for the workstation. |
| Option C: | A physical address that is assigned by the manufacturer. |
| Option D: | A physical address that is randomly assigned each time the computer is started. |
| 11. | An address in a block is 180.8.17.9. Find the first address and last address in the block. |
| Option A: | 180.8.0.0 and 180.8.255.255 |
| Option B: | 180.8.1.0 and 180.8.255.0 |
| Option C: | 180.8.1.1 and 180.8.255.255 |
| Option D: | 180.8.0.0 and 180.8.1.1 |
| 12 | Dustin langth in classical addressing can be |
| 12. | Prefix length in classless addressing can be |
| Option A: | 1 to 16 |
| Option B: | 1 to 32 |
| Option C: | 1 to 24 1 to 8 |
| Option D: | 1 10 0 |
| 13. | What is the SUBNET mask for a class C Network? |
| Option A: | 255.0.0.0 |
| Option B: | 255.255.255.0 |
| Option C: | 255.255.0.0 |
| opnon o. | |

| Option D: | 255.255.255 |
|-----------|---|
| | |
| 14. | Which of the following is the Protocol of Application layer? |
| Option A: | TCP |
| Option B: | UDP |
| Option C: | SCTP |
| Option D: | DNS |
| 1.7 | |
| 15. | To deliver a message to the correct application program running on a host, the address must be consulted. |
| Option A: | IP |
| Option B: | MAC |
| Option C: | Port |
| Option D: | Physical |
| 1 | |
| 16. | What is the hexadecimal equivalent of the Ethernet address 01011010 00010001 |
| | 01010101 00011000 10111010 111111111? |
| Option A: | 5A:88:AA:18:55:F0 |
| Option B: | 5A:81:BA:81:AA:0F |
| Option C: | 5A:18:5A:18:55:0F |
| Option D: | 5A:11:55:18:BA:FF |
| | |
| 17. | User datagram protocol is called connectionless because |
| Option A: | all UDP packets are treated independently by transport layer |
| Option B: | it sends data as a stream of related packets |
| Option C: | it is received in the same order as sent order |
| Option D: | it sends data very quickly |
| | |
| 18. | Which connector does the STP cable use? |
| Option A: | BNC |
| Option B: | RJ-11 |
| Option C: | RJ-45 |
| Option D: | RJ-69 |
| | |
| 19. | The default connection type used by HTTP is |
| Option A: | Persistent |
| Option B: | Non-persistent |
| Option C: | Can be either persistent or non-persistent depending on connection request |
| Option D: | reference request |
| | |
| 20. | Simple mail transfer protocol (SMTP) utilizes as the transport layer protocol |
| | for electronic mail transfer. |
| Option A: | TCP |
| Option B: | UDP |
| Option C: | IP SCTP |
| Option D: | SCTP |

| Q.2 | Solve any Two Questions out of Three. | 10 marks each) |
|-----|--|----------------|
| C | | |
| A | What are the functions of layers in the OSI model? | |
| В | Classify the various multiple access methods and explain detail. | n CSMA-CD in |
| С | What is traffic shaping? Explain leaky bucket technique an technique of traffic shaping. | d Token Bucket |

| Q.3 | Solve any Two Questions out of Three. (10 marks each) |
|-----|---|
| | Define the utilization or efficiency of the line and derive the expression for stop and wait flow control. Calculate the maximum link utilization for following cases: |
| | i)stop and wait flow control |
| A | ii) Sliding window flow control with window sizes of 4 & 7 |
| | Link specification: |
| | Frame length=5000 bits/frame |
| | Velocity of propagation= 2x10 ⁸ m/s, Link distance=30km, Data rate=50 Mbps |
| В | 1 8 2 7 3 9 11 8 4 14 4 8 7 6 10 |
| | Using Dijkstra's shortest path algorithm, find the shortest path |
| | An organization is granted a block of addresses with the beginning address 14.24.74.0/24. The organization needs to have 3 subblocks of addresses to use in its three subnets as shown below: |
| С | □One subblock of 120 addresses. |
| C | □One subblock of 60 addresses. |
| | □One subblock of 10 addresses |
| | From above information, design the subnetworks and find the information about each network. |

Examination 2021 under Cluster 06

(Lead College: Vidyavardhini's College of Engg Tech)

Examinations Commencing from June 01, 2021

Program: **Electronics Engineering**Curriculum Scheme: Rev 2016
Examination: TE Semester VI

Course Code: ELX603 Course Name: VLSI Design

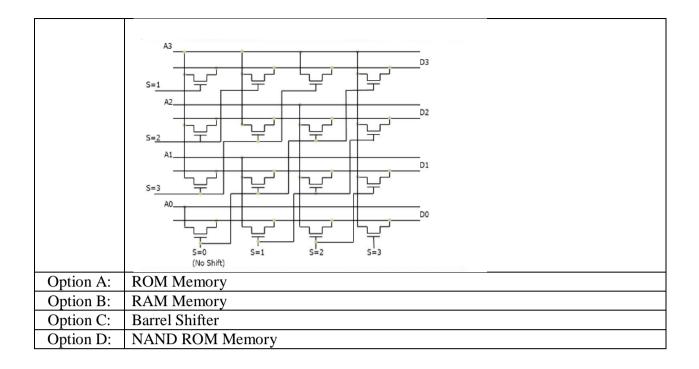
Time: 2 hour Max. Marks: 80

| Q1. | Choose the correct option for following questions. All the Questions are compulsory and carry equal marks |
|-----------|---|
| | |
| 1. | The CMOS logic circuit for NOR gate is: |
| Option A: | A P Y |
| Option B: | A B Y |
| Option C: | A B Y |

| 2. In Pseudo-nMOS inverter logic, the gate of pmos transistor operates is: - Option A: Connected to VDD Option B: Grounded Option C: Connected to gate of nmos transistor Option D: Kept floated 3. | Option D: | |
|--|-----------|--|
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| Option A: | | Y |
| Option A: Connected to VDD Option B: grounded Option C: Connected to gate of nmos transistor Option D: Kept floated 3. | | لط لط ا |
| Option A: Connected to VDD Option B: grounded Option C: Connected to gate of nmos transistor Option D: Kept floated 3. | | , , , , , , , , , , , , , , , , , , , |
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| Option A: | 2. | In Pseudo-nMOS inverter logic, the gate of pmos transistor operates is: - |
| Option B: | Option A: | |
| Option C: Connected to gate of nmos transistor Option D: Kept floated 3. | | grounded |
| Option D: Kept floated 3. | | |
| 3. Option A: XNOR Option B: XOR Option D: OR 4. Sense amplifiers are primarily used in: - Option A: Memory circuits Option B: Adder Circuits Option D: Option C: Ander Circuits Option D: Option C: Manchester carry chain adders Option D: Operational Amplifier 5. In 6 T SRAM Cell the core is made up of how many inverters Option A: 4 Option B: 2 Option C: 5 Option C: 5 Option D: 6 6. The capacitance used in 1 T DRAM cell is: - Option A: Normal Electrolytic Capacitor Option B: Diffusion Capacitance Option C: MOSFET capacitance Option D: Trench Capacitance Option A: When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | | |
| C-A indicates complement of A and —B indicates complement of B) Above Circuit is Option A: XNOR Option B: XOR Option C: AND Option D: OR 4. Sense amplifiers are primarily used in: - Option A: Memory circuits Option B: Adder Circuits Option B: Adder Circuits Option C: Manchester carry chain adders Option D: Operational Amplifier 5. In 6 T SRAM Cell the core is made up of how many inverters Option A: 4 Option B: 2 Option C: 5 Option C: 5 Option D: 6 6. The capacitance used in 1 T DRAM cell is: - Option A: Normal Electrolytic Capacitor Option B: Diffusion Capacitance Option C: MOSFET capacitance Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | • | |
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| Option B: 2 Option C: 5 Option D: 6 6. The capacitance used in 1 T DRAM cell is: - Option A: Normal Electrolytic Capacitor Option B: Diffusion Capacitance Option C: MOSFET capacitance Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | | |
| Option C: 5 Option D: 6 6. The capacitance used in 1 T DRAM cell is: - Option A: Normal Electrolytic Capacitor Option B: Diffusion Capacitance Option C: MOSFET capacitance Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | | |
| Option D: 6 6. The capacitance used in 1 T DRAM cell is: - Option A: Normal Electrolytic Capacitor Option B: Diffusion Capacitance Option C: MOSFET capacitance Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | | |
| 6. The capacitance used in 1 T DRAM cell is: - Option A: Normal Electrolytic Capacitor Option B: Diffusion Capacitance Option C: MOSFET capacitance Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | | |
| Option A: Normal Electrolytic Capacitor Option B: Diffusion Capacitance Option C: MOSFET capacitance Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | Priori D. | |
| Option A: Normal Electrolytic Capacitor Option B: Diffusion Capacitance Option C: MOSFET capacitance Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | 6. | The capacitance used in 1 T DRAM cell is: - |
| Option B: Diffusion Capacitance Option C: MOSFET capacitance Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | | |
| Option C: MOSFET capacitance Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | | |
| Option D: Trench Capacitance 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | | |
| 7. When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. Option A: saturation | | WOSFET capacitance |
| transistors are in region. Option A: saturation | | |
| transistors are in region. Option A: saturation | 7 | |
| Option A: saturation | / . | Trench Capacitance |
| | 7. | Trench Capacitance When a CMOS inverter withdraws maximum current from the supply, the two |
| Option B: linear | | Trench Capacitance When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. |
| Option C: non saturation | | Trench Capacitance When a CMOS inverter withdraws maximum current from the supply, the two transistors are in region. |

| Option D: | cut-off |
|-----------|--|
| | |
| 8. | The Manchester Carry-Chain Adder is having a part of transistors that are used to implement the carry chain. |
| Option A: | PASS |
| Option B: | PNP |
| Option C: | NPN |
| Option D: | BJT |
| • | |
| 9. | For the body effect to occur in a MOSFET, substrate is biased with respect to |
| Option A: | Gate |
| Option B: | Drain |
| Option C: | Source |
| Option D: | Body |
| | |
| 10. | Ids is to length L of the channel. |
| Option A: | Square law |
| Option B: | Logarithmically |
| Option C: | Directly Proportional |
| Option D: | Inversely Proportional |
| | |
| 11. | . А В |
| | |
| | · · · - · • · · · · · · - · · · · · · · · · · |
| | |
| | 1 |
| | The circuit shows two pass transistors in series. Find the value of Y? |
| Option A: | Y=A.B |
| Option B: | Y=A+B |
| Option C: | Y=A.A |
| Option D: | Y=B.B |
| 10 | ECD whom a manufactural of the |
| 12. | ESD phenomenon stands for |
| Option A: | Electron Source Detection |
| Option B: | Electron Static Discharge |
| Option C: | Electrostatic Discharge |
| Option D: | Discharged Capacitor |
| 13. | The device in which NMOS and PMOS pair wired in parallel with their sources |
| 13. | connected and drains connected is called as |
| Option A: | Transmission Gate |
| Option B: | CMOS inverter |
| Option C: | Pseudo NMOS inverter |
| Option C: | Manchester circuit |
| Орион Б. | Municipester circuit |
| 14. | H-tree Distribution to all chip level circuits is used to avoid following error: - |
| Option A: | Clock skew |
| Option B: | Clock jitter |
| Option C: | Charge sharing |
| | |

| Option D: | Charge leakage |
|-----------|--|
| • | |
| 15. | Charge Sharing and Charge Leakage Problem in Domino cascade circuits can be |
| | removed by |
| Option A: | Dynamic Circuit |
| Option B: | Single FET charge keeper circuit. |
| Option C: | Static CMOS Circuit |
| Option D: | Clocked CMOS circuits. |
| | |
| 16. | The refresh frequency in DRAM cell is |
| Option A: | $f_{\text{refresh}}=1/2t_{\text{h}}$ |
| Option B: | $f_{\text{refresh}}=1/3t_{\text{h}}$ |
| Option C: | $f_{\text{refresh}}=1/t_{\text{h}}$ |
| Option D: | $f_{\text{refresh}}=1/4t_{\text{h}}$ |
| 1.7 | |
| 17. | |
| | R2 R2 |
| | |
| | vi vout |
| | C2 C2 |
| | |
| | For the above circuit vi is the input voltage ,vout is the output voltage of the |
| | circuit. By Elmore's formula find out the time constant of the circuit. |
| Option A: | R_2C_2 |
| Option B: | $3R_2C_2$ |
| Option C: | $4R_2C_2$ |
| Option D: | $2R_2C_2$ |
| option D. | |
| 18. | When Kn>Kp, Threshold voltage of CMOS Inverter move closer to |
| Option A: | Zero |
| Option B: | Infinity |
| Option C: | Midpoint Value |
| Option D: | Supply Voltage |
| • | |
| 19. | In Integrated Chips circuits are connected to each other mostly by: - |
| Option A: | connection |
| Option B: | Interconnect |
| Option C: | wires |
| Option D: | PCB |
| | |
| 20. | Find the name of below diagram |



subjective/descriptive questions

| Q2 | Solve any Four out of Six 5 marks each |
|------------|--|
| (20 Marks) | |
| A | What is Scaling in VLSI Technology? List the types of scaling and explain any one in detail. |
| В | Explain CMOS inverter characteristics mentioning it's all regions of operation. |
| С | Implement $Z=(\overline{A+B+C})\overline{DE}$ using CMOS static circuit. |
| D | Draw Schematic of 6T SRAM Cell and Explain it's working |
| Е | Compare pass transistor and transmission gate, list two advantages of transmission gate. |
| F | Write short note on Importance of low power design in VLSI circuits. |

| Q3. (20 Marks Each) | | |
|---------------------|--|--------------|
| A | Solve any Two out of Three 5 | marks each |
| i. | Write short note on Interconnect scaling and crosstalk of the ir | nterconnect. |
| ii. | Draw J-K Flipflop using CMOS and explain its operation. | |
| iii. | Explain concept of precharge and evaluation in Dynamic CMC | OS circuits |
| В | Solve any One out of Two | 0 marks each |
| i. | Consider a CMOS Inverter circuit with following parameters | |
| | VTO,n=0.6 v , VTO,p= -0.7v | |
| | μ nCox=60 μ A/V ² , (W/L) n=8 | |
| | μ pCox=25 μ A/V ² , (W/L) p=12 | |
| | Calculate noise margin, If the power supply voltage VDD=3.3 | V |
| ii. | Compare Ripple carry adder and Carry Lookahead adder, Exp. | lain 4-bit |
| | CLA adder circuit. | |

Examination 2021 under Cluster 06

(Lead College: Vidyavardhini's College of Engg Tech)

Examinations Commencing from June 01, 2021

Program: **Electronics Engineering**Curriculum Scheme: Rev 2016
Examination: TE Semester VI

Course Code: ELX 604 and Course Name: Signals and Systems

Time: 2 hour Max. Marks: 80

| Q1. | Choose the correct option for following questions. All the Questions are compulsory and carry equal marks |
|-----------|--|
| | |
| 1. | Determine the signal is periodic or not. If a signal is periodic, specify it's fundamental period of signal $x(n) = e^{j7\pi n}$ |
| Option A: | x(n) is an Aperiodic signal |
| Option B: | x(n) is Periodic with fundamental period N=2 samples/cycle |
| Option C: | x(n) is Periodic with fundamental period N=7 samples/cycle |
| Option D: | x(n) is Periodic with fundamental period N=14 samples/cycle |
| | |
| 2. | What is the area of a Unit Impulse function? |
| Option A: | Zero |
| Option B: | Half of Unity |
| Option C: | Depends on the function |
| Option D: | Unity |
| | |
| 3. | Convolution of the sequences of $x_1(n) = x_2(n) = \{1,1,1\}$? |
| Option A: | {1,1,1,1} |
| Option B: | {1,2,3,2,1} |
| Option C: | {1,2,3,1} |
| Option D: | {1,2,2,1} |
| 4. | A discrete-time system with input $x(n)$ and $y(n)$ related by $y(n) = n[x(n)]$ |
| Option A: | linear ,time varying, and stable |
| Option B: | non-linear, time invariant, and unstable |
| Option C: | non-linear, time varying, and stable |
| Option D: | linear, time varying, and unstable |
| | |
| 5. | What is the Nyquist rate of the following signal |
| | $x(t) = 3\cos(50\pi t) + 10\sin(300\pi t) - \cos(100\pi t)$? |
| Option A: | 50 Hz |
| Option B: | 100 Hz |
| Option C: | 200 Hz |
| Option D: | 300Hz |
| | |

| 6. | What is the condition for consolity in Lanlace domain? |
|-----------|---|
| | What is the condition for causality in Laplace domain? |
| Option A: | ROC should be to the right of right most pole |
| Option B: | ROC should be to the right of right most zero |
| Option C: | ROC should be to the right of left most pole |
| Option D: | All the zeros should be in the right half of the s plane |
| 7. | Which type of system response to its input represents the zero value of its initial condition? |
| Option A: | Zero state response |
| Option B: | Zero input response |
| Option C: | Total response |
| Option C: | Natural response |
| Option D. | Tvaturai response |
| 8. | What is the z-transform of $x(n-1)$ if $x(n)$ has z-transform $X(Z)$? |
| Option A: | ZX(Z) |
| Option B: | $\begin{bmatrix} -X(Z) \end{bmatrix} \begin{bmatrix} Z^1 \end{bmatrix}$ |
| Option C: | $ [X(-Z)][Z^{\wedge}(-1)] $ |
| Option C: | $[X(Z)][Z^{(-1)}]$ |
| Option D. | |
| 9. | A finite- length signal has X (z) = $0.5+0.2 z^{-1} + 0.7 z^{-2} + 0.5 z^{-3}$; its ROC is |
| Option A: | The entire $z - plane$ except $z = 0$ |
| Option B: | Outside the unit circle |
| Option C: | Inside the unit circle |
| Option C: | On the unit circle |
| Option D. | On the unit chee |
| 10. | The convolution property of the z-transforms states that the inverse z – transform of H (z) X (z) is given by |
| Option A: | $\sum_{k=0}^{n-1} h(k)x(n-k)$ |
| Option B: | $\sum_{k=0}^{\infty} h(k)x(k-n)$ |
| Option C: | $\sum_{k=-\infty}^{\infty} h(k)x(n-k)$ |
| Option D: | $\sum_{k=-\infty}^{0} h(n-k)x(n)$ |
| 11. | Find the Laplace Transform of $y(t) = y(t)$ $y(t) = y(t)$ |
| Option A: | Find the Laplace Transform of $x(t) = u(t) - u(t-a)$ |
| Option A. | $\frac{1-e^{as}}{s}$ |
| Option B: | 1 |
| F | |
| | s-a |
| Option C: | $1-e^{-as}$ |
| | S |
| | 1 |

| Option D: | 1 |
|-----------|--|
| | $\frac{1}{s+a}$ |
| | s + a |
| 12. | Find the initial and final values for the following function |
| 12. | Find the initial and final values for the following function |
| | $X(s) = \frac{s+5}{s^2+3s+2}$ |
| | |
| Option A: | initial value =0 and final value= 1 |
| Option B: | initial value = 1 and final value = 0 |
| Option C: | initial value = 5 and final value = 3 |
| Option D: | initial value = 3 and final value= 5 |
| 13. | The trigonometric Fourier series of a periodic time function can have only |
| Option A: | Only cosine terms |
| Option B: | Only sine terms |
| Option C: | Both cosine and sine terms |
| Option D: | Dc and cosine terms |
| | |
| 14. | Which among the below mentioned transform pairs is/are formed between the auto-correlation function and the energy spectral density, in accordance to the property of Energy Spectral Density (ESD)? |
| Option A: | Laplace Transform |
| Option B: | Z-Transform |
| Option C: | Fourier Transform |
| Option D: | Wavelet Transform |
| | |
| 15. | The Fourier transform of the signal $\delta(t+1) + \delta(t-1)$ is |
| Option A: | $2/(1+j\omega)$ |
| Option B: | $2/(1-j\omega)$ |
| Option C: | $2\cos\omega$ |
| Option D: | $2 \sin \omega$ |
| | |
| 16. | Duality Theorem / Property of Fourier Transform states that |
| Option A: | Shape of signal in time domain & shape of spectrum can be interchangeable |
| Option B: | Shape of signal in frequency domain & shape of spectrum can be interchangeable |
| Option C: | Shape of signal in time domain & shape of spectrum can never be interchangeable |
| Option D: | Shape of signal in frequency domain & shape of spectrum can never be interchangeable |
| 17. | Which theorem states that the total average power of a periodic signal is equal to |
| 17. | the sum of average powers of the individual Fourier coefficients? |
| Option A: | Parseval's Theorem |
| Option B: | Rayleigh's Theorem |
| Option C: | Thevenin's Theorem |
| Option D: | Norton's Theorem |
| - F | |
| 18. | Choose the correct expression for Fourier series coefficient Ck in terms of the discrete signal x(n). |

| Ontion A. | W 4 |
|-----------|---|
| Option A: | $\frac{1}{N}\sum_{n=0}^{N-1}x(n)e^{\frac{j2\pi nk}{N}}$ |
| Option B: | $\frac{1}{N}\sum_{n=0}^{N-1}x(n)e^{\frac{-j2\pi nk}{N}}$ |
| Option C: | $\frac{1}{N} \sum_{n=0}^{N+1} x(n) e^{\frac{j2\pi nk}{N}}$ |
| Option D: | $\frac{1}{N} \sum_{n=0}^{N+1} x(n) e^{\frac{-j2\pi nk}{N}}$ |
| 10 | |
| 19. | The discrete time signal a ⁿ .u(n) will have alternate positive and negative |
| | amplitudes decaying with time for following case. |
| Option A: | -1 <a<0; and="" n<0<="" td=""></a<0;> |
| Option B: | -1 <a<0; and="" n="">0</a<0;> |
| Option C: | 0 <a<1; and="" n<0<="" td=""></a<1;> |
| Option D: | 0 <a<1; and="" n="">0</a<1;> |
| | |
| 20. | The Fourier transform of the signal sgn(t) is |
| Option A: | $-2j\omega$ |
| Option B: | $4j\omega$ |
| Option C: | $2/(j\omega)$ |
| Option D: | $(1+j\omega)$ |

| Q2. | (20 Marks) |
|--------------|--|
| | |
| \mathbf{A} | Solve any Two 5 marks each |
| i. | Determine the power and energy of the following continuous time signal $x(t)=e^{-at}\ u(t)$ |
| ii. | Check for the Dynamicity, Linearity, Shift Variant , Causality and Stability $y(t) = x(2t)$ |
| iii. | Obtain the Fourier transforms and spectrums of the signal $x(t) = \cos w_o t$ |
| В | Solve any One 10 marks each |
| i. | Find the inverse Laplace transform of the function $X(S) = \frac{3s+7}{(s^2-2S-3)}$ For ROCs of i) Re (s) > 3 ii) Re (s) < -1 iii) -1 < Re (s) < 3 |
| ii. | Perform the convolution of $x_1(t) = e^{-3t} u(t)$ and $x_2(t) = t u(t)$ Using |

mathematical method and also by graphical method.

| Q3. | (20 Marks) |
|------|---|
| | |
| A | Solve any Two 5 marks each |
| i. | Find the DTFT of discrete time signal $x(n) = a^n u(n)$ for $-1 < a < 1$. |
| ii. | Determine the z-transform of |
| | $x(n) = (1/2)^n u(n) + 2^n u(n)$. Find the ROC and draw the locations of poles and zeros in the z-plane. |
| iii. | Write the relationship between z-transform and discrete time fourier transform. |
| В | Solve any One 10 marks each |
| i. | Find the inverse z- transform of |
| | $X(Z) = \frac{1}{1 - 1.5z^{-1} + 0.5z^{-2}}$ |
| | For ROCs of i) ROC: $ (Z) > 1$ |
| | ii) ROC: $ (Z) < 0.5$ |
| | iii) ROC: $0.5 < (Z) < 1$ |
| ii. | Determine DTFS for the sequence $x(n) = 4 \cos(\frac{\pi n}{2})$ |

Examination 2021 under Cluster 06

(Lead College: Vidyavardhini's College of Engg Tech)

Examinations Commencing from June 01, 2021

Program: **Electronics Engineering** Curriculum Scheme: Rev 2016 (CBCGS)

Examination: TE Semester VI Course Code: **ELXDLO6023** and Course Name: **Wireless Communication**

Time: 2 hour Max. Marks: 80

| Q1. | Choose the correct option for following questions. All the Questions are compulsory and carry equal marks |
|-----------|--|
| | |
| 1. | What must be designed to separate the transmit & receive signal at mobile subscriber unit. |
| Option A: | Antenna |
| Option B: | Duplexer |
| Option C: | Transceiver |
| Option D: | Control Unit |
| 2. | Formulate the system capacity, if a mobile communication system has allocated number of 800 voice channels. If the service area is divided into 20 cells with a frequency reuse factor of 4. |
| Option A: | 800 |
| Option B: | 3200 |
| Option C: | 4000 |
| Option D: | 16000 |
| | |
| 3. | For a given frequency reuse ratio of 8 and the cell radius of 0.8 km, the distance between nearest cochannel cells is |
| Option A: | 6.4 km |
| Option B: | 0.8 km |
| Option C: | 0.1 km |
| Option D: | 8.8 km |
| | |
| 4. | To examine the measure of the ability of a mobile subscriber to access a cellular |
| | system during the busiest hour is |
| Option A: | circuit merit level |
| Option B: | mean opinion score |
| Option C: | grade of service |
| Option D: | service quality |
| 5. | Two main reasons that contribute to the rapid fluctuations of the signal amplitudein mobile communications are |
| Option A: | Multipath fading and Doppler effect |
| Option B: | Reflection and Refraction |
| Option C: | Diffraction and Scattering |
| Option D: | Blocking and Shadowing |

| 6. | In the development of base station transmitter operates at 900 MHz carrier frequency. For a mobile moving at a speed of 72 Km/h in a direction perpendicular to the direction of arrival of the transmitted signal, the received |
|-----------|--|
| | carrier frequency is |
| Option A: | 899.9994 MHz |
| Option B: | 900.00006 MHz |
| Option C: | 900.00003 MHz |
| Option D: | 900 MHz |
| 7. | When 2 mobile subscribers are located at distance of 100 meters & 1 km apart |
| | from cell site resp. then by what amount the received signal strength differs? |
| | (assuming other parameters are constant). |
| Option A: | 20 dB |
| Option B: | 40 dB |
| Option C: | 80 dB |
| Option D: | 100 dB |
| 8. | The guard time between the time slots in TDMA frame helps in minimizing the |
| | interference due toalong different radio paths in the wireless channel. |
| Option A: | propagation delays |
| Option B: | adjacent channel |
| Option C: | multipath fading |
| Option D: | timing inaccuracies |
| 9. | To synthesize the increment in bandwidth of message signa, the deciding factor |
| | is |
| Option A: | PN Sequence |
| Option B: | Gold sequence |
| Option C: | Spread spectrum |
| Option D: | Processing gain |
| 10. | X-OR addition of 2 m sequence PN generators is nothing but |
| Option A: | propagation delay generator |
| Option B: | spectrum modulation |
| Option C: | golden ration generator |
| Option D: | gold sequence generator |
| 11. | To organize high spectrum efficiency and constant amplitude in GSM, the |
| | modulation technique used is |
| Option A: | FSK |
| Option B: | QPSK |
| Option C: | GMSK |
| Option D: | OFDM |
| 12. | To facilitate the identity of mobile phone device, the MSC uses the database as |
| Option A: | HLR |

| Option B: | VLR | |
|-----------|---|--|
| Option C: | AuC | |
| Option D: | EIR | |
| орион В. | | |
| 13. | Considering Coded data packets in GSM, compute the net data rate (data plus | |
| | signaling) and the effective transmission rate of a 9,600 bps GSM data service. | |
| Option A: | 9600 bps | |
| Option B: | 22.8 kbps | |
| Option C: | 33.854 kbps | |
| Option D: | 13 kbps | |
| 14. | If the trailing bits, stealing bits, guard bits, and training bits in a GSM frame are | |
| 1 | considered as overhead, and the rest of the bits as data, then what is the | |
| | percentage overhead in a GSM frame? | |
| Option A: | 57.14 % | |
| Option B: | 70.166 % | |
| Option C: | 91 % | |
| Option D: | 27 % | |
| 1 | | |
| 15. | To illustrate the user occupying (a single) time slot has to wait for time duration | |
| | of between two successive transmissions | |
| Option A: | 577 μs | |
| Option B: | 4.615 ms | |
| Option C: | 120 ms | |
| Option D: | 6.12 s | |
| | | |
| 16. | While design, the effect of spread spectrum modulation is that the bandwidth of | |
| | the spreaded signal | |
| Option A: | remains constant | |
| Option B: | increases significantly | |
| Option C: | increases marginally | |
| Option D: | decreases | |
| 1.7 | | |
| 17. | How much bandwidth is occupied in selection of each carrier of IS-95 standard | |
| Option A: | 25 KHz | |
| Option B: | 30 KHz | |
| Option C: | 200 KHz | |
| Option D: | 1250KHz | |
| 18. | Cdma2000-1xRTT system supports a typical throughput of up to per | |
| | mobile user. | |
| Option A: | 115kbps | |
| Option B: | 144 kbps | |
| Option C: | 384 kbps | |
| Option D: | 2 mbps | |
| | | |
| 19. | In closed loop power control, the base station sends power control messages to | |
| | the mobile user about once every | |

| Option A: | 1 ms |
|-----------|---|
| Option B: | 10 ms |
| Option C: | 100 ms |
| Option D: | 1 s |
| | |
| 20. | The logical control channel specified on the reverse link in W-CDMA system is |
| | which channel? |
| Option A: | Sync |
| Option B: | Access |
| Option C: | Paging |
| Option D: | pilot |

| Q2 | | | |
|------|---|--|--|
| A | Solve any Two 5 marks each | | |
| i. | Distinguish between frequency division duplexing & time division duplexing | | |
| ii. | Describe various factors influencing small scale fading | | |
| iii. | Discuss in brief about TDMA frame structure & Efficiency of TDMA. | | |
| В | Solve any One 10 marks each | | |
| i. | Explain GSM Network architecture with neat block diagram. | | |
| | Compute the longest time over which a mobile station would have to wait in | | |
| | order to determine the frame number being transmitted by GSM cell-site. | | |
| ii. | Illustrate the function of GPRS architecture in brief. | | |
| | A CDMA system has a bandwidth of 1.25 MHz and transmits baseband data at | | |
| | 9.6 kbps rate. If 40 number of users can simultaneously establish communication | | |
| | links, what is the bandwidth efficiency of the system? | | |

| Q3 | | |
|------|--|--|
| A | Solve any Two 5 marks each | |
| i. | Describe the concept of frequency reuse, define cluster. | |
| ii. | Explain the types of small-scale fading. | |
| iii. | Discuss about direct sequence spread spectrum transmitter & receiver with | |
| | neat block diagram. | |
| В | Solve any One 10 marks each | |
| i. | Explain hand off in GSM, Illustrate types of GSM hand off in GSM. If the | |
| | trailing bits, stealing bits, guard bits, and training bits in a GSM frame are | |
| | considered as overhead, and the rest of the bits as data, then what is the | |
| | percentage overhead in a GSM frame? | |
| ii. | Distinguish between W-CDMA and IS-95 CDMA. | |
| | Determine the maximum raw instantaneous data rate that can be provided to a | |
| | single user in EDGE, assuming that a single time slot on a single GSM channel | |
| | is available. | |

Examination 2021 under Cluster 06

(Lead College: Vidyavardhini's College of Engg Tech)

Examinations Commencing from June 01, 2021Program: **Electronics Engineering**

Curriculum Scheme: Rev 2016 Examination: TE Semester VI

Course Code: ELXDLO6024 and Course Name: Computer Organization and Architecture Time: 2 hour Max. Marks: 80

| Q1. | Choose the correct option for following questions. All the Questions are compulsor and carry equal marks | | |
|-----------|--|--|--|
| | and carry equal marks | | |
| 1. | Which of the following Special purpose register holds the address of next instructions to | | |
| 1. | be executed? | | |
| Option A: | Program Counter | | |
| Option B: | Instruction Register | | |
| Option C: | MAR | | |
| Option D: | Base Register | | |
| | | | |
| 2. | Booth's Multiplier | | |
| Option A: | reduces the number of partial products | | |
| Option B: | increases the number of partial products | | |
| Option C: | multiplies the number of partial products | | |
| Option D: | divides the partial products | | |
| • | | | |
| 3. | Bias value for single precision and double precision representation is & | | |
| Option A: | 128, 1024 | | |
| Option B: | 127, 1023 | | |
| Option C: | 256, 512 | | |
| Option D: | 32, 64 | | |
| | | | |
| 4. | A set of microinstructions for a single machine instruction is called | | |
| Option A: | Program | | |
| Option B: | Command | | |
| Option C: | Micro program | | |
| Option D: | Micro command | | |
| | | | |
| 5. | Full form of MFLOPS is | | |
| Option A: | Millions of Fixed Point Operations Per Second | | |
| Option B: | Millions of Floating Point Operations Per Second | | |
| Option C: | Millions of Floating Point Opcodes Per Second | | |
| Option D: | Millions of Flip/Flops Operations Per Second | | |
| | | | |
| 6. | A micro-programmed control unit | | |
| Option A: | faster than a hard-wired control unit | | |
| Option B: | facilitates easy implementation of new instructions | | |
| Option C: | useful when very small programs are to be run | | |
| Option D: | usually refers to the control unit of microprocessor. | | |
| | | | |
| 7. | How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes? | | |
| Option A: | 8 | | |
| Option B: | 16 | | |

| Option C: | 2 | | |
|-----------|---|--|--|
| Option D: | 4 | | |
| Option D. | | | |
| 8. | Which of the following is not a write policy to avoid Cache Coherence? | | |
| Option A: | Write through | | |
| Option B: | Write within | | |
| Option C: | Write back | | |
| Option D: | Buffered write | | |
| Option D. | Burrered write | | |
| 9. | Which algorithm chooses the page that has not been used for the longest period of time | | |
| | whenever the page required to be replaced? | | |
| Option A: | First in first out algorithm | | |
| Option B: | Additional reference bit algorithm | | |
| Option C: | Least recently used algorithm | | |
| Option D: | Counting based page replacement algorithm | | |
| | | | |
| 10. | What are the five main components of a computer system | | |
| Option A: | CPU,CD-ROM, Mouse, Keyboard, Sound Card | | |
| Option B: | Memory ,Video card, Monitor, Software, Hardware | | |
| Option C: | Modem, Keyboard, Word Processor, Printer, Screen | | |
| Option D: | CPU, Memory ,System bus ,Input, Output | | |
| | | | |
| 11. | Cache memory works on the principle of | | |
| Option A: | Locality of Memory | | |
| Option B: | Locality of reference | | |
| Option C: | Locality of data | | |
| Option D: | Locality of reference and memory | | |
| | | | |
| 12. | Hidden bus arbitration is feature of | | |
| Option A: | MOD BUS | | |
| Option B: | CAN BUS | | |
| Option C: | PCI BUS | | |
| Option D: | ISA BUS | | |
| | | | |
| 13. | SIMD stands for | | |
| Option A: | Single information Multiple Design | | |
| Option B: | Single Instruction Multiple Data | | |
| Option C: | Single Instructions Multiple Design | | |
| Option D: | Single Information Multiple document | | |
| 1 4 | Which of the following processes has a first langth of instruction of | | |
| 14. | Which of the following processor has a fixed length of instructions? | | |
| Option A: | CISC | | |
| Option B: | RISC | | |
| Option C: | EPIC | | |
| Option D: | Multi core | | |
| 15. | The concept of pipelining is most effective performance if the tasks being performed in | | |
| 13. | different stages | | |
| Option A: | Require different amount of time | | |
| Option B: | Require about the same amount of time | | |
| Option C: | Require different amount of time with time difference between any two tasks being same | | |
| Option C: | Require different amount with time difference between any two tasks being different | | |
| option D. | 1.040.10 chilotone amount with time difference octween any two tasks being different | | |
| 16. | The set of loosely connected computers are called as | | |
| Option A: | LAN | | |
| Option A. | LAN | | |

| 0 5 | YYYAAY | |
|-----------|--|--|
| Option B: | WAN | |
| Option C: | Workstation | |
| Option D: | Cluster | |
| | | |
| 17. | An instruction pipeline can be implemented by means of | |
| Option A: | LIFO Buffer | |
| Option B: | FIFO Buffer | |
| Option C: | Stack | |
| Option D: | Both LIFO Buffer and FIFO Buffer | |
| | | |
| 18. | The Unit of data Exchange between Cache and Main Memory is known as | |
| Option A: | Cache size | |
| Option B: | Block size | |
| Option C: | Page size | |
| Option D: | Segment size | |
| | | |
| 19. | Hazards due to resource conflict are called as | |
| Option A: | Data Hazard | |
| Option B: | Control Hazard | |
| Option C: | Structural Hazard | |
| Option D: | Both Data Hazard and Control Hazard | |
| | | |
| 20. | The following sequence of virtual page numbers is encountered in the course of | |
| | execution on a computer with virtual memory: 3 4 2 6 4 7 1 3 2 6 3 5 1 2 3 Assume that a | |
| | least recently used page replacement policy. Find out the Page Hit Ratio with main | |
| | memory with Page capacity $n = 4$. Assume that main memory is initially empty. | |
| Option A: | 0.22 | |
| Option B: | 0.10 | |
| Option C: | 0.20 | |
| Option D: | 0.16 | |

| Q2 | | |
|------------|--|---------------|
| (20 Marks) | | |
| A | Solve any Two 5 marks each | |
| i. | Draw and explain instruction state diagram(without interrupt). | |
| ii. | Explain different write policy methods. | |
| iii. | Explain SRAM structure and working. | |
| В | Solve any One | 10 marks each |
| i. | Discuss system buses in detail. Highlight PCI bus and its operatio | n in detail. |
| ii. | Discuss Hardwired and Micro-programmed Control unit in detail. | |
| | | |
| Q3 | | |
| (20 Marks) | | |
| A | Solve any Two out of three | 5 marks each |
| i. | Write short notes on GPU. | |
| ii. | Discuss paging concept in short. | |
| iii. | Discuss I/O handling techniques. (any two techniques) | |
| В | Solve any One out of two | 10 marks each |
| i. | Discuss parallel processing and pipelining in detail. | |
| ii. | Explain Flynn's classification in detail with suitable diagrams. | |