[**Total Marks: 80**]

(3 Hours)

NB: 1) Question No. 1 is compulsory.
2) Attempt any 3 questions out of remaining questions.
3) Figures on the right hand side indicate full marks.
4) Assume Suitable data if necessary

Q1 Answer any **four**

a) Explain different commutation techniques for SCR. Draw current commutation circuit **20**
b) Draw and explain gate characteristics.
c) What is the need of freewheeling diode in rectifiers? Explain with suitable diagrams.
d) Explain Type B DC-DC converter.
e) Explain why harmonic neutralization is necessary in the output of inverter.

Q2 a) Draw and explain single phase fully controlled converter with RL load .Draw load current, Load voltage, input voltage and gating signal for $\alpha = 60^0$ **10**

b) Explain the working of three phase bridge inverter in 120^0 conduction mode with circuit diagram and waveforms. **10**

Q3 a) Draw and Explain dynamic characteristics of thyristor. **10**

b) Explain working principle of 1 Φ cyclo converter with circuit diagram and waveforms. **10**

Q4 a) A single phase fully controlled converter is operated from 230V, 50 Hz ac supply. The load resistance is 10 Ω. The average output voltage is 10% of max possible average output voltage **10**

Calculate- i) Firing angle
ii) RMS and Average output current
iii) Efficiency

b) Draw and explain the working of 3Φ fully controlled rectifier with neat circuit diagram and waveforms. **10**

Q5 a) Draw and explain AC voltage control circuit using DIAC and TRIAC. Draw the waveforms with $\alpha = 60^0$. **10**

b) Draw and explain Buck converter with waveforms. Also derive the expression for output voltage. **10**

[PTO...

Q6 Write short notes on (Any **Four**) **20**

a) Compare IGBT, MOSFET.

b) Protection circuits for SCR.

c) Driver circuits for power transistors.

d) Various PWM techniques.

e) Ramp and Pedestal control triggering.

Time: 03 Hours **Marks: 80**

N.B.

1) Question number ONE is compulsory.

2) Attempt any THREE questions from remaining questions.

3) All questions carry equal marks.

Q1] Answer any four questions

a) Compare Butterworth and Chebyshev filtres. 5

b) Compare FIR and IIR filters. 5

c) Compute the DFT of the sequence x(n)={ 0, 1, 2, 1} 5

d) What is Frequency prewarping in Bilinear transformation method? Why it is required. 5

e) Explain the speed improvement in calculating the DFT using FFT. 5

Q2] a) Find DFT of the following sequence using DIT FFT algorithm. 10

$x(n) = \{1, 1, 1, 1, 1, 1, 1, 0\}$

b) Find the circular convolution of the two finite duration sequences 10

$x1(n) = \{1, -1, -2, 3, -1\}$ $x2(n) = \{1, 2, 3\}$.

Q3] a) Design a Butterworth digital IIRlow pass filter using Bilinear transformation by taking T=1 second, to satisfy the following specifications. $0.707 \le |H(e^{jw}| \le 1.0 \; : \; 0 \le w \le 0.2\pi$

$|H(e^{jw}| \le 0.08 \; : \; 0.4\pi \le w \le \pi$ 10

b) Given that, H(s) = 1/(S+1). By impulse invariant method, obtain the digital filter transfer function y(n). 10

Q4] a) Explain different addressing modes of TMS 320 c67XX. 10

b) Explain VLIW architecture in detail. 10

Q5] a) Design a linear phase FIR highpass filter using hamming window, with a cutoff frequency, $w_c = 0.8\pi$rad/sample and N = 7 10

b) Explain Frequency sampling method of designing FIR filter? 10

Q6] Write short notes on (any two)

a) Effect of quantization in computation of DFT. 10
b) Application of DFT to Radar signal Processing. 10
c) Gibs Phenomenon. 10

Duration: 2 Hours **Marks-40**

Note:

i. Q.1 is compulsory
ii. Attempt any three questions from remaining five.
iii. Each question carries equal marks.

1. Answer any five.

a. Which are the components of IT Infra? **2**
b. Write any four top security concerns. **2**
c. Explain optical storage. **2**
d. Explain World Wide Web. **2**
e. What do you mean by cabling? **2**
f. Define Information architecture. **2**
g. Differentiate between single mode and multimode fiber. **2**

2.

a. Define topology. Explain any three common topologies. **5**
b. Explain wireless LAN technologies with their advantages. **5**

3.

a. Explain Simple Network Management Protocol **5**
b. Explain seven layer OSI stack. **5**

4.

a. Illustrate Enterprise Resource planning (ERP) and its need in detail. **5**
b. Write a short note on following web authoring tools. **5**
i) SGML
ii) HTML

5.

a. Which are the three main types of storage? Write a short note on each. **5**
b. Explain Password management System **5**

6. Write a note on following terms related to IT audit. **10**
i) Information audit.
ii) Audit schedule
iii) Audit plan
iv) Audit preparation
v) Internal audit.

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Q. P. Code: 36415

Time: 3 hours **Total Marks: 80**

Note: 1) Question No.1 is compulsory.
2) Attempt any three questions from remaining five questions.
3) Assume suitable data if necessary.
4) Figures to the right indicate full marks.

Q.1) Explain in brief
- a) Integral controller 5M
- b) Telemetry 5M
- c) I-P converter 5M
- d) Pneumatic logic gates 5M

Q.2) a) Compare conventional and smart transmitters. Explain the working of DP transmitter. 10M

b) What are the different characteristics of data loggers? Draw the block diagram of data logger and explain its working? 10M

Q.3) a) Explain compressed air receiver unit. What are the different control strategies for air receiver unit? 10M

b) Explain detail cylinder construction with its dynamics. 10M

Q.4) a) What is the need of composite controller? Explain PI controller in detail. 10M

b) Give the classification of compressors. Explain any two rotary compressors with diagram. 10M

Q.5) a) Explain loading of valves in pump application with diagram. 10M

b) Give the classification of control valve based on characteristic, plug design etc. 10M

Q.6) a) Give the comparisons of electrical, hydraulic and pneumatic systems. 10M

b) Brief the classification of hydraulic pumps. Draw neat sketches of any three hydraulic pumps and explain the working. 10M

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Duration: 3 Hours **Marks: 80**

N.B : (1) Question No.1 is compulsory.

(2) Attempt any three questions from remaining questions.

(3) Figures to the right indicate full marks.

Q1(a) Explain restoring division algorithm and draw its flowchart. 5

(b) Describe the concept of Nanoprogramming. 5

(c) Compare paging and segmentation. 5

(d) Draw the register structure of IA-32 family 5

Q2 (a)What is the necessity of replacement algorithm? Explain how pages are replaced between cache memory and main memory using replacement policies :

(i) LRU (ii) FIFO 10

(b)Explain the structure of serial and parallel ports. What are the methods to access it? 10

Q3 (a) Explain in detail any one hardwired technique of control unit design. 10

(b) Explain various DMA transfer modes with diagrams. 10

Q4 (a) Explain the advantages of pipelining. Explain various types of pipeline hazards and solutions to prevent them. 10

(b) Explain concept of cache memory with reference to principle of locality and Hit ratio Draw and explain different architectures of cache memory. 10

Q5 (a) What are different addressing modes of IA-32 family? Explain with examples. 10

(b) Explain single bus and multiple bus organization. 10

Q6 (a) Explain the Virtual Address to Physical address Translation for the following specifications Virtual Memory=128k and Main Memory=32k, page size = 1k. Illustrate Page Fault with the help of a example. 10

(b) Explain execution of a complete instruction with details. How are branch instructions executed? Use Single Bus organization. 10

Q. P. Code: 37282

[Time: 3 Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B:
1. **Question 1 is compulsory**
2. **Solve any tree out of reaming.**
3. **Assume suitable data if necessary**
4. **Draw proper diagrams**

Q.1 Solve any four. 20

a. What are different MOS capacitances? Explain in brief.
b. Implement Y=$\overline{(A+B).(C+D)}$ Using pseudo NMOS logic.
c. What is low power design in VLSI circuits?
d. Define scaling. Explain significance of scaling in VLSI circuits.
e. Explain working of 1-T DRAM cell.

Q.2
a. Explain CMOS inverter characteristics mentioning all regions of operation. What is the effect of changing W/L ratio on it? Explain with example. 10

b. Implement 4:1 mux using pass transistor logic. Explain advantages of using transmission gates. 10

Q.3
a. Derive equations for noise margin for CMOS invertor. 10
b. Explain working of 6-T SRAM cell. 10

Q.4
a. Explain clock generation networks and distribution networks used in VLSI circuits. 10
b. What is fast adder? Explain any one schemes for fast adder. 10

Q.5
a. Explain pseudo NMOS logic and hence implement 2 I/P NAND gate. 10
b. Explain various ESD protection schemes. 10

Q. 6 Write a short note on. 20

a. Barrel shifter
b. NOR based ROM array
c. Interconnect scaling
d. Level-1 and Level-2 MOS models.