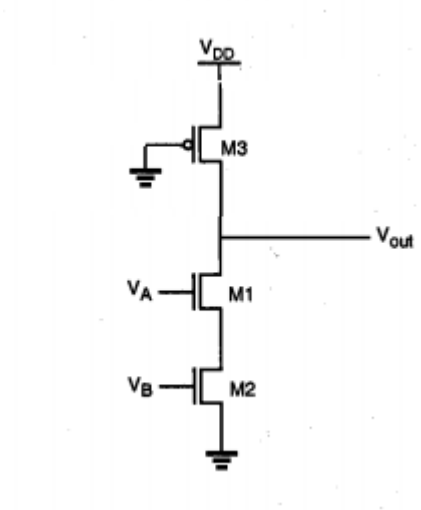
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Power dissipation, after applying constant field scaling
Option A:	decreases by factor of S
Option B:	increases by factor of S^3
Option C:	increases by factor of S
Option D:	decreases by factor of S^2
2.	In case of CMOS Inverter, Critical Voltage V_{IL} is given by
Option A:	$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD/2} + K_R V_{T0,n}}{1+K_n}$
Option B:	$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + K_R V_{T0,p}}{1 + K_R}$
Option C:	$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + K_R V_{T0,n}}{1+K_R}$
Option D:	$V_{IL} = \frac{2V_{out} + V_{T0,n} - V_{DD} + K_R V_{T0,p}}{1+K_R}$
3.	Consider a CMOS Inverter circuit with the following parameters: $V_{DD} = 3.3\,V$, $V_{T0,n} = 0.6\,V$, $V_{T0,p} = -0.7\,V$ $K_n = 200\,\mu A/V^2$, $K_p = 80\,\mu A/V^2$ Calculate V_{IH}
Option A:	1.08 V
Option B:	1.55 V
Option C:	3.3 V
Option D:	0 V
4.	Identify type of Circuit 

Option A:	2 input pseudo nmos NOR gate
Option B:	2 input pseudo nmos NAND gate
Option C:	2 input CMOS OR gate
Option D:	2 input CMOS AND gate
5.	What are the limitations of Dynamic CMOS logic?
Option A:	charge latching
Option B:	charge leakage and sharing
Option C:	charge distribution
Option D:	leakage current
6.	How many TGs are required for Implementation of XOR gate? (TG means Transmission Gates)
Option A:	2
Option B:	8
Option C:	7
Option D:	4
7.	Static CMOS logic is an ----------.
Option A:	ratioed logic
Option B:	non-ratioed logic
Option C:	negative logic
Option D:	positive logic
8.	Sense amplifier is used to----------.
Option A:	sense small voltage difference at bit-line
Option B:	sense bit-line capacitance
Option C:	sense impedance of bit-line
Option D:	sense resistance of bit-line
9.	In a 1T DRAM, information is stored in----------.
Option A:	latch
Option B:	parasitic capacitor
Option C:	trench capacitor
Option D:	virtual capacitor
10.	---------- are designed to overcome the latency introduced by the rippling effect of the carry bits.
Option A:	Ripple carry adders
Option B:	Carry look-ahead (CLA) adders
Option C:	Ripple carry and sum look-ahead adders
Option D:	Half and full adders

Q2. **(20 Marks Each)**	**Solve any Two Questions out of Three 10 marks each**
A	*Write a note on MOSFET Capacitances.*
B	*Derive the expression of all critical voltages for CMOS inverter.*
C	*Explain interconnect scaling and crosstalk.*
Q3. **(20 Marks Each)**	**Solve any Two Questions out of Three 10 marks each**
A	*Explain Dynamic and Domino logic used for MOS circuit design.*
B	*Implement 4:1MUX using pass transistor and Transmission gates.*
C	*Explain working of JK flipflop using static CMOS design logic.*
Q4. **(20 Marks Each)**	**Solve any Two Questions out of Three 10 marks each**
A	*What is Carry select adder? Explain it's working.*
B	*Write a note on array multiplier.*
C	*What is SRAM? Explain the stability of 6T SRAM cell.*