T.E. (Sem-VI) CBSGS 9/6/2015
Electronics Engineering
MITM

QP Code : 5057

(2 Hours) **[Total Marks : 40**

N.B. : (1) Question No. one is compulsory.
(2) Attempt any three from remaining five questions

1. Answer any five.
   - **a.** Define OSI layers. **2**
   - **b.** Write a small note on E-business. **2**
   - **c.** What is data mining? **2**
   - **d.** Define intranet and explain it. **2**
   - **e.** Write a note on structured cabling **2**
   - **f.** What is data quality problem. **2**
   - **g.** What is E-governance framework. **2**

2.
   - **a.** Explain open source software with examples. **5**
   - **b.** Write a note on mesh topology and star topology. **5**

3.
   - **a.** Explain the different types of operating systems. **5**
   - **b.** Write a note on password management system. **5**

4.
   - **a.** Explain the following terms related to storage. **5**
     - i) Online storage
     - ii) Near line storage
     - iii) Offline storage
   - **b.** Write a detailed note on Simple Network Management Protocol (SNMP). **5**

5.
   - **a.** Explain Enterprise Resource Planning (ERP)and its need. **5**
   - **b.** Explain web browsers with different examples. **5**

6. Write a note on following terms related to security Infrastructure **10**
   - i) RFID Systems.
   - ii) Video surveillance
   - iii) Biometric systems
   - iv) End point security
   - v) IP-CCTV

1

TE Sem VI (CBGS) (EXTC)

DSPP

3/6/15

Q.P. Code : **5056**

(3 Hours) [Total Marks : 80

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **three** questions from remaining questions.
(3) **Assume** suitable data wherever **necessary**.

1. (a) State and explain relation between DTFS, DFT and ZT. 4
(b) Explain the term linear phase & state its importance in digital filters. 4
(c) What is need of DSP processor whent high speed processor are available ? 4
(d) What is meant by limit cycle in IIR system. Give example. 4
(e) Explain different signal processing operations involved in subband coding. 4

2. (a) Design 6^{th} order linear phase LPF with cut of frequency $\pi/2$ using Blackman window function. 10
(b) Explain Gibb's phenomenon. State it's significance in FIR filter design. 10

3. (a) Given $H(S)=\frac{1}{(s+1)(s+3)}$, T = 2 seconds Design digital IIR filter using BLT method. Explain Frequency warping in BLT. 10
(b) A digital system is characterized by difference Equation, 10
$y(n) = 0.9\ y\ (n-1) + x\ (n)$ Explain the limit cycles generated in the output & determine the deadband of system when input $x(n)= 0$ and $y(n-1) = 12$

4. (a) Compute DFT of sequence $x(n)\cos\left(\frac{n\pi}{2}\right)$, $N = 4$ using DIF-FFT algorithm 5
(b) Find IDFT of $x\ (k) = \{3, (2 + j), 1\ , (2 - j)\}$ 5
(c) Find DTFS of $x\ (n) = \{0, 1, 2, 3\}$ with period $N = 4$. State time shifting property of DTFS. 10

5. (a) Explain how higher throughout is obtained in DSP using VLIW architecture. 10
(b) In a recursive system defined by Transfer function. 10

$$H(z)=\frac{1}{\left(1-0.35z^{-1}\right)\left(1-0.62z^{-1}\right)}$$

Assume that products are rounded to 4-bits including sign bit and the product range is -1 to 1. Find output roundoff noise power in direct form realization.

6. (a) Explain different addressing modes of TMS320C67XX DSP processor 10
(b) What are the sailent features of TMS320C67XX family of DSP processors. 10

T.E. (sem VI) (CBGS) Electronics Engg 28/5/2015

Power Electronics. I

QP Code : 5052

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **three** questions out of remaining **five** question.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) Draw and explain V-I characteristics of SCR. **5**
   (b) What is the need of frewheeling diode in controlled rectifier. Explain with example. **5**
   (c) What do you understand by $\frac{di}{dt}$ and $\frac{dv}{dt}$ rating of SCR. **5**
   (d) Explain the principle step down clopper. State load voltage equation. **5**

2. (a) Explain half controlled rectifier using SCR. Draw waveforms and derive the relation for output load voltage. **10**
   (b) Draw and explain single phase full bridge inverter. Draw waveforms. **10**

3. (a) Single phase half bridge invertor has a resistive load of 3Ω and the dc input voltage E_{dc} = 50 V. Calculate
   (i) RMS output voltage at the fundamental frequency
   (ii) Output power P_0
   (iii) The average and peak current of each thyristor.
   (iv) The peak reverse blocking voltage of each thyristor.

4. (a) Explain the working of single phase to single phase cycloconverter with purely resistive load. Draw circuit diagram and waveforms. **10**
   (b) The input voltage to the buck-boost convertor is E_{dc} = 14V. The duty cycle a = 0.6 and the switching frequency is 25 KHz. The inductance L = 180 μH and filter capacitance C = 220 μH. The average load current Io = 1.5 A. calculate **10**
   (a) The average o/p voltage E_0
   (b) The peak-to-peak output voltage ripplea ΔV_c
   (c) The peak-to-peak current of inductor Δ I
   (d) The peak current of the device Ip

[TURN OVER

5.	(a)	Explain circuit diagram and working of three phase inverter 180^0 conduction mode with resistive load.	10
	(b)	Diffrentiate between symmetrical and asymmetrical IGBT.	5
	(c)	Draw and explain switching characteristics of IGBT.	5
6.	(a)	Explain the voltage control technique in inverter using sinusoidal pwm method. Justify the use of it reduces harmonics.	10
	(b)	Draw and explain dual convertor with all four quadrants of operation.	5
	(c)	Define forced communication. Explain Class D communication with respect to circuit diagram, working and waveforms.	5

TE. SEM VII (CBSGS) - ETRX

C.O.

May 2015

Q.P. Code : **5049**

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. 1 is compulsory.
(2) Attempt **any three** questions out of **remaining five** questions.
(3) Assume suitable data **wherever** necessary.
(4) Figures to the right indicate **full marks**.

1 (a) Write microinstructions for executing instruction Add Ro, [R3] in three bus architecture processor. **5**

(b) Write a note on nanoprogramming. **5**

(c) Differentiate SRAM and DRAM. **5**

(d) What is parallel processing? **5**

2. (a) Draw flowchart for non-restoring division. Solve (8) ÷ (3) using non-restoring division method. **10**

(b) Differentiate between Horizontal and vertical micro architecture. **10**

3. (a) Consider main memory size is three pages. Following page address trace is generated by execution of a program **10**

2 3 2 1 5 2 4 5 3 2

Assume main memory is cleared initially. Find page hit ratio by

(i) FIFO (ii) LRU replacement scheme.

(b) What is microprogramming? Draw and explain microprogrammed control unit. **10**

4. (a) What is virtual memory? How paging is useful in implementing virtual memory? **10**

(b) State the advancements in arithmetic and logical instructions supported by IA-32 architecture. Describe five floating point arithmetic instructions in IA-32. **10**

5. (a) Explain various DMA transfer modes in brief with examples. **10**

(b) Explain various types of hazards in pipelined processors with example. Also propose solution for each type. **10**

6. (a) What are different I/O access methods? Explain in detail. **10**

(b) Write short notes on :- **5**

(i) Cache coherency **5**

(ii) RISC and CISC architectures.

JP-Con. 10227-15.

T.E. Sem VI (CBGS) ETRX. 18/5/15

Adv. Instrumentation System

QP Code : 5047

(3 Hours) [Total Marks: 80]

N. B.: (1) Question No. 1 is compulsory.
(2) Attempt any three questions from remaining five questions.
(3) Assume suitable data if necessary.
(4) Figures to the right indicate full marks.

1. (a) With neat block diagram, explain the working of multichannel data acquisition system. **10**

   (b) Compare an electrical, pneumatic and hydraulic systems. **10**

2. (a) Explain flow characteristics of globe control valves. **10**

   (b) What is necessity of valve positioner? Explain any one type of valve positioner. **10**

3. (a) Explain the working of pneumatic to electrical converter. **10**

   (b) What is need of tuning of controller? Explain any one method of tuning of PID controller. **10**

4. (a) Explain flapper nozzle system. Explain any two applications of flapper nozzle System. **10**

   (b) With neat block diagram explain working of telemetry system. **10**

5. (a) Compare conventional and smart transmitters. **10**

   (b) Draw and explain inherent and installed characteristics of control valves. **10**

6. (a) With neat diagram, explain speed control circuit for hydraulic actuator. **10**

   (b) Explain the working of electronic DP transmitter. **10**

****

(78)

T.E. (ETRX) – VI

12/5/2015

Basic VLSI Design

QP Code : 5043

(3 Hours) **[Total Marks : 80**

N.B. (1) Question No. **1** is **compulsory**.
(2) Solve any **three** questions from **remaining** questions.
(3) Assume suitable **data** if **necessary**.

1. Solve any **four** of the following :—
   (a) Explain the effect on drain current due to channel length modulation and velocity saturation. **5**
   (b) Implement using CMOS inverters. **5**

$$F = \overline{A \cdot B} + C$$

   (c) Draw voltage transfer characteristic for CMOS inverter and explain all regions. **5**
   (d) Give the read and write stability criteria for 6T RAM if the pull up transistors and replaced by resistors. **5**
   (e) Explain low power design considerations. **5**

2. (a) Compare pass transistor logic, NMOS logic and CMOS logic. **10**
   (b) For equal rise and tall delay five assume $\mu_n = 2\,\mu_p$ drew an inverter equivalent circuit of 3 i/p NAND and 2 i/p XOR. **10**

3. (a) Compare constant voltage and constant field scaling with their merits and demerits. **10**
   (b) Write short note on clock generation, stabilization and distribution. **10**

4. (a) Explain concept of carry look ahead adder with equation and how does it achieve better speed compared to ripple carry Adder. **10**
   (b) Consider a CMOS inverter with following parameters **10**

Nmos V to, n = 0·6 V μ_n Cox = 60 $\mu A / V^2$ and $\left(W/L\right)_n = 8$

p mos V to, p = –0·7 V μ_n Cox = 25 $\mu A / V^2$ and $\left(W/L\right)_p = 12$

Calculate the noise margin and switching threshold (V_{Th}) of this circuit, $V_{DD} = 3V$.

5. (a) Implement 4 : 1 multiplexer using pass transistor logic. **10**
   (b) Explain concept of charge sharing and charge leakage. **10**

[TURN OVER

6. Write a short notes on any **three** of the following :— 20

(a) Sense amplifier

(b) Array multiplier (4 × 4)

(c) CMOS Latch up and it's prevention.

(d) Resistance and capacitance estimation.
