T.E- VI - ETRX - CBSGS. 14/12/15

Digital Signal Processing & Processors.

Dec-2015

Q.P. Code : 6432

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No.1 is compulsory.
(2) Answer any three questions from remaining five question.
(3) All questions carry equal marks.

1. (a) Justify: In impulse invariance transformation method there is many to one mapping of poles from s-plane to z-plane. 5
(b) Find the number of computations required to compute 32 point DFT using direct calculation and by using FFT algorithm. Also find the computational complexity. 5
(c) Compare DSP processor and microprocessor. 5
(d) Compare fixed point arithmetic and floating point arithmetic. 5

2. (a) Find the DFT of the following sequence using Radix 2 DIF FFT algorithm 10
$x(n) = \{1, 2, 3, 4, 4, 3, 2, 1\}$
(b) Compute the circular convolution of the sequences using DFT and IDFT approach. 10
$x_1(n)$ $\{1, 2, 0\}$
$x_2(n) = \{2, 2, 1, 1\}$

3. (a) Design a Low pass FIR filter with 11 coefficients for the following specifications. Passband frequency edge = 0.25KHz and sampling frequency = 1 KHz 10
Use rectangular window in the design.
(b) Explain frequency sampling method of designing FIR filter. 10

4. (a) Use bilinear transformation to obtain a digital filter of notch frequency 75Hz and sampling frequency of 200 Hz, for a given normalized second order filter having transfer function $H(S) = \frac{S^2+1}{S^2+S+1}$ 10
(b) Design a Butterworth lowpass filter to meet the following specifications. 10
Passband gain = 0.89
Passband frequency edge = 30Hz
Attenuation = 0.20
Stopband edge = 75Hz

5. (a) Explain with neat diagram architecture of TMS320C67XX DSP processor. 10

(b) Explain the applications of the DSP processor in following fields. 10

(i) Radar signal processing

(ii) Speech recognition.

6. (a) Draw the quantization noise model for second order system. 10

$$H(z) = \frac{1}{1 - 2r\cos\theta z^{-1} + r^2 z^{-2}}$$

find the steady state output noise variance.

(b) Explain the following terms.

(i) Dead band 3

(ii) Limit cycle oscillations 3

(iii) Addressing modes of TMS320C67XX processor. 4

T.E – VI – ETRX – CBSGS.

Power Electronics – I

Dec – 2015.

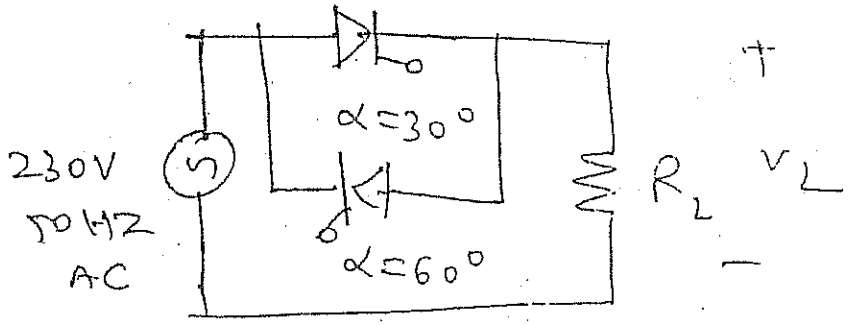
8/12/15

QP Code : **6390**

(3 Hours) [Total Marks : 80

N. B. : (1) Question No. 1 is **compulsory**.
(2) Solve any **three** questions out of remaining **five** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) Draw and explaian gate characteristics of SCR. 5
(b) Differentiate between symmetrical IGBT and asymmetrical IGBT 5
(c) Draw output voltage waveform for the circuit given below. Draw waveform with scale. 5



(d) Explain in brief why harmonic neutrilisation is necessary in the output of inverter. 5

2. (a) Explain the working of dual converter with all far avadronts of operation. Draw circuit diagram and waveforms. 10
(b) Draw and explain of working of buck boost converter with the help of circuit diagram and waveforms. Derive the relation for output voltage. 10

3. (a) Explain three phase bridge inverter with 120° conduction mode. Draw circuit diagram and waveforms. 10
(b) With the help of circuit diagram and waveforms explain bi-directional AC control circuit using TRAC & DIAC. 10

4. (a) Explain semiconverter circuit for the conversion of AC to DC. Draw waveforms for $\alpha = 60°$. Explain how it eliminates the need of prewheeling diode in case of R-L Load to increase the power factor. 10
(b) Explain class D commutation circuit with the help of circuit diagram and waveforms. 10

[TURN OVER

5. (a) Explain in detail SOA of MOSFET. 5
(b) Explain multiple pulse width modulation to control the output of inverter with sine wave as a reference signal. 10
(c) What do you understand by cycloconverter. Draw single phase cycloconverter with circuit diagram and waveforms. 5

6. (a) Draw and explain three phase fully controlled bridge rectifier with R load in contineous mode. Derive the relation for output voltage. 10
(b) A single phase semiconverter is operated from 120V 50 HZ ac. supply. The load resistance is 10 ohm. If the average output voltage is 25% of the maximum possible average output voltage. Determine. 10
(i) Firing angle
(ii) RMS and average output current
(iii) RMS and average thysistor current.

TE - VI - ETRX - CBSGS
Computer Organization
Nov-Dec '2015

2|12|15

QP Code : 6348

[Total Marks: 80]

(3 Hours)

N.B. : (1) Question No. 1 is compulsory.
(2) Attempt any three questions from remaining questions.
(2) All questions carry equal marks.
(3) Figures to the right indicate full marks.

Q1.

a) What is parallel processing?
b) Write short note on nanoprogramming.
c) Compare RISC and CISC machines.
d) What is effect of multiple data paths in design of processor .

Q2.

a) Explain Booth's Algorithm . Solve (+7) * (-5) using Booth's Algorithm.
b) Compare Hardwired control unit and Microprogrammed control unit.

Q3.

a)Consider main memory size as three pages . Following page address trace is generated by execution of a program

2 3 2 2 1 5 4 2 3 1 2 4
4 4 2

Assume main memory is cleared initially. Find page hit ratio by
1)FIFO 2) LRU 3) LFU replacement policies.

b) Explain IA-32 architecture in detail.

Q4.

a) Explain Cache memory and describe Cache mapping techniques.
b) What is bus arbitration? What are different methods to resolve bus arbitration.

Q5.

a)Explain advantages of interrupt driven I/O over polling. Explain interrupt driven I/O access with one example.

b) Draw and explain microprogrammed control unit for multiplier.

Q6. Write short note on any four

a. Pipeline Hazards.
b. Memory Hierarchy
c. Restoring Division algorithm.
d. 8085 addressing modes
e. Arithmetic Instructions in IA-32 architecture.

T.E - VI - ETRX - CBSGS.
Advanced Instrumentation System.
Nov - Dec '2015.

26/11/15

QP Code : **6305**

(3 Hours) [Total Marks : 80

N.B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **three** questions from remaining **five** questions.
(3) Assume **suitable data** if **necessary**.
(4) **Figures** to the **right** indicate **full** marks.

1. (a) What is need of tuning of PID controller ? Explain process reaction curve method for tuning of PID controller. 10
   (b) With neat diagram, explain working of telemetry system. 10

2. (a) Explain installed and inherent characteristics of control valves. 10
   (b) Explain construction and working of single and double acting actuators. 10

3. (a) Compare conventional and smart transmitters. 10
   (b) With neat block diagram, explain the working of electrical to pneumatic converter. 10

4. (a) Explain the working of electronic DP transmitter. 10
   (b) Explain flapper-nozzle system. Explain any two applications of flapper-nozzle system for industrial use. 10

5. (a) Explain the installation procedure of control valve. 10
   (b) With neat diagram, explain the parallel form of PID controller. 10

6. (a) What is necessity of valve positioner ? Explain anyone valve positioner in detail. 10
   (b) With neat diagram, explain the instrument air system. 10

———v———

T.E- VI – ETRX- CBSGS
Basic VLSI Design
NOV-Dec 2015

19/11/15

QP Code : 6263

(3 Hours) [Total Marks : 80

N.B. : (1) Question No.1 is compulsory.
(2) Attempt any three out of remaining.
(3) Assume suitable data wherever required.

1. (a) Draw CMOS implementation of D Flip Flop. 20
(b) Implement $y=\overline{A+B\cdot C}$ using dynamic CMOS logic.
(c) Explain latchup in CMOS inverter.
(d) Define scaling. Explain significance of scaling in VLSI circuits.

2. (a) Draw CLA (carry lookahead adder) carry chain using. 10
(i) Static CMOS logic
(ii) Dynamic CMOS logic
(iii) Pseudo NMOS logic
(b) Draw 1T DRAM cell and explain it's read write and refresh operation. 10

3. (a) Explain clock generation networks and distribution networks used in VLSI circuits. 10
(b) Give and explain CMOS input & output protection circuits. 10

4. (a) Implement 4x4 barrel shifter using transmission gate. Explain various operation using the same. 10
(b) Explain programming techniques used for EEPROM. 10

5 (a) What are the drawbacks of dynamic CMOS logic. Show the modification in dynamic CMOS logic to over come it's drawback. 10
(b) Explain operating regions of CMOS inverter with equations. 10

6. Write short notes on. 20
(a) Interconnect scaling
(b) Cross talk
(c) Array multiplier
