## **BE Electronics Engineering**

Curriculum Scheme: Revised 2016

Examination: Second Year Semester IV

Course Code: ELX403 and Course Name: Microprocessors & Applications

iline: I nour	IVIAX. IVIAI KS. :	

Note to the students: - All the Questions are compulsory and carry equal marks.

Q1.	8086 is a bit processor
Option A:	8
Option B:	16
Option C:	4
Option D:	24
Q2.	Which is also called multiprocessor mode?
Option A:	Simple
Option B:	Minimum
Option C:	Maximum
Option D:	Complex
Q3.	Carry is a bit flag
Option A:	1
Option B:	2
Option C:	8
Option D:	16
Q4.	In max mode, control bus signal So, S1 and S2 are sent out in
	form
Option A:	Shared
Option B:	Unshared
Option C:	Decoded
Option D:	Encoded
Q5.	In minimum mode, is used to produce read and write signals
Option A:	8255
Option B:	8282
Option C:	8286
Option D:	74138
Q6.	How many 8286 transreceivers are used in minimum mode?
Option A:	2
Option B:	3

Option C:	1
Option D:	4
Q7.	Which device provides Clock signals to 8086?
Option A:	8284
Option B:	8255
Option C:	8282
Option D:	8085
Q8.	The addressing mode of ADD AX,BX is
Option A:	Direct Addressing Mode
Option B:	Indirect Addressing Mode
Option C:	Register Addressing Mode
Option D:	Immediate Addressing Mode
Q9.	What is the size of the biggest instruction in 8086?
Option A:	2 bytes
Option B:	6 bytes
Option C:	3 bytes
Option D:	4 bytes
Q10.	Which of the followings is not an Arithmetic Instruction?
Option A:	INC
Option B:	CMP
Option C:	DEC
Option D:	ROL
Q11.	What does STC instruction do
Option A:	Clear Carry
Option B:	Set Direction
Option C:	Seize Carry
Option D:	Set Carry
Q12.	How many Hardware Interrupts are there in 8086?
Option A:	256
Option B:	5
Option C:	2
Option D:	255
Q13.	A program for interrupt is called as
Option A:	Interrupt Program
Option B:	Interrupt Service Routine

Option C:	Sub program
Option D:	Function
Q14.	8087 connection to 8086, to enable thebank of memory
	pins are to be connected.
Option A:	Lower, BHE
Option B:	Upper, BHE
Option C:	Lower, INT
Option D:	Upper, INT.
Q15.	How many address lines are required to interface 22KB memory ship
	How many address lines are required to interface 32KB memory chip  10 address lines
Option A:	11 address lines
Option B:	18 address lines
Option C:	15 address lines
Option D:	15 address lifles
Q16.	Port C of 8255 can function independently as
Option A:	input port
Option B:	output port
Option C:	either input or output ports
Option D:	both input and output ports
Q17.	8259 can operate in how many modes
Option A:	2
Option B:	1
Option C:	5
Option D:	6
Q18.	How many peripherals can 8237 DMA controller handle at one time?
Option A:	1
Option B:	2
Option C:	4
Option D:	3
орион Б.	3
Q19.	Which addressing line is used along with BHE, for interfacing operations?
Option A:	AO
Option B:	A1
Option C:	A2
Option D:	A3
Q20.	Which memory is used in Pentium Processors
Option A:	Bus Memory
Option B:	Static Memory
Option C:	Dynamic Memory
Option D:	Virtual Memory
	3   Pag

Q21.	Who is the manufacturer of Pentium Processors
Option A:	IBM
Option B:	Cisco
Option C:	HCL
Option D:	Intel
Q22.	How much minimum Virtual memory can be accessed by Pentium Processors?
Option A:	1MB
Option B:	1GB
Option C:	2GB
Option D:	256GB
Q23.	Number of address lines in Pentium Processor is
Option A:	16
Option B:	20
Option C:	32
Option D:	64
Q24.	During execution of one instruction, during pipelining, the next instruction is
	stored in
Option A:	BIU
Option B:	CPU
Option C:	Control Unit
Option D:	Memory unit
Q25.	The execution in which the consecutive instruction execution in a sequential flow
	is hampered is
Option A:	Speculative Execution
Option B:	Out of turn execution
Option C:	Dual instruction
Option D:	Branch instruction