University of Mumbai
Examination 2021
Program: **Electronics Engineering**
Curriculum Scheme: Rev 2016
Examination: ME Semester I(CBCGS)
Course Code: ELXC1012 and Course Name: Mixed Signal VLSI Design

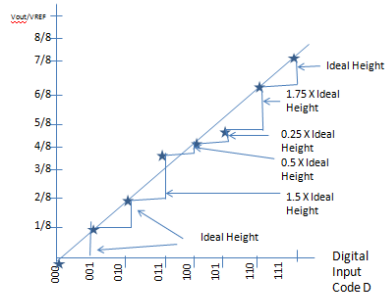
Time: 2 hour Max. Marks: 80

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	Condition for MOSFET in saturation region ?
Option A:	Vds = Vgs
Option B:	Vgs = Vth
Option C:	Vds >= Vgs - Vth
Option D:	Vds <= Vgs - Vth
Q2.	The voltage Vgs after which MOSFET will turn on ?
Option A:	Cutoff Voltage
Option B:	Threshold Voltage
Option C:	Pinch off Voltage
Option D:	Cut in Voltage
Q3.	RAM circuit which is used in cache memories
Option A:	SRAM
Option B:	DRAM
Option C:	RAM
Option D:	ROM
Q4.	Which RAM circuit is faster
Option A:	DRAM
Option B:	RAM
Option C:	ROM
Option D:	SRAM
Q5.	RAM which needs refreshing cycle is
Option A:	ROM
Option B:	PROM
Option C:	FLASH
Option D:	DRAM
Q6.	EXPAND DLL
Option A:	Phase Locked Loop
Option B:	Dephase Locked Loop
Option C:	Delay Locked Loop
Option D:	Digital Locked Loop

Q7.	Expand the term VCO
Option A:	Voltage Oscillator
Option B:	Voltage Controlled Oscillator
Option C:	Voltage Carrier Oscillator
Option D:	Volt Control Operator
Q8.	_____ gate is used as a phase detector
Option A:	OR gate
Option B:	XOR gate
Option C:	AND gate
Option D:	NOR gate
Q9.	NSA Stand for
Option A:	NMOS Sense Amplifier
Option B:	NMOS State Amplifier
Option C:	NMOS Select Amplifier
Option D:	NMOS Sense Angle
Q10.	In a RAM array architecture column is calculated by
Option A:	Ccol = Colisub
Option B:	Ccol = (no. of word lines) X (cap of MOS S/D) + Ccolisub
Option C:	Ccol = Cap of MOS S/D
Option D:	Ccol = Rcol +Wcol
Q11.	State 2 problems in Sense amplifier design
Option A:	Kickback noise and Clock Circuit
Option B:	Kickback noise and Clock feed through
Option C:	Kickback noise and Carrier noise
Option D:	Clock feed through and operational noise
Q12.	In switched capacitor sampling circuit ----------is used as a switch
Option A:	BJT
Option B:	Diode
Option C:	MOSFET
Option D:	FET
Q13.	Which noise is created in sampling circuit
Option A:	White noise
Option B:	Jitter
Option C:	Thermal Noise
Option D:	Flicker Noise
Q14.	Technique to reduce the effect of charge injection
Option A:	Add a dummy switch
Option B:	Add noise
Option C:	add JFET

Option D:	add BJT
Q15.	Coupling occurs due to ---------- capacitances between the interconnect lines
Option A:	Lower band
Option B:	Coupling
Option C:	Parasitic
Option D:	upper band
Q16.	Propagation delay is defined as
Option A:	tPHL =0.7(R1+R2)Cload
Option B:	tPHL =0.7(R1*R2)Cload
Option C:	tPHL =0.7(R1)Cload
Option D:	tPHL =0.7(R2)Cload
Q17.	Power consumption is defined as
Option A:	Pavg = n Vdd x Iavg
Option B:	Pavg = n Vdd
Option C:	Pavg = n Vdd
Option D:	Pavg = n Vdd x Iavg
Q18.	A circuit used to clean up an interconnecting signal
Option A:	Schmitt Trigger
Option B:	sample and hold
Option C:	invertiing amplifier
Option D:	oscillator
Q19.	3 types of multivibrator circuits
Option A:	monostable, bistable, tristable
Option B:	monostable, quasistable, tristable
Option C:	monostable, distable, tristable
Option D:	monostable, distable, tristable
Q20.	State the tecnique used to minimize charge sharing
Option A:	Bootstrapping
Option B:	charge sharing
Option C:	addition of capacitance
Option D:	jitter

Q2 **(20 Marks Each)**	**Solve any Two out of Three 10 marks each**
A	Draw and Explain ROM array using NOR-NOR logic?
B	Determine the DNL for the 3-bit nonideal DAC whose transfer curve is shown in the following figure.Assume that VREF=5V . 
C	Explain non-ideal effects in PLL

Q3. (20 Marks Each)	Solve any Two out of Three 10 marks each
A	What is the “lock Acquisition “problem in type I PLL and how it can be overcome?
B	Explain any charge pump (voltage generator) circuit used to generate a voltage greater than VDD
C	Write short note on: F-N model of memory Clock feed through Ring oscillator Charge pump PLL