Curriculum Scheme: Revised 2016 (CBCGS)

Examination: Second Year Semester IV

Course Code: ELX404 Course Name: Digital System Design

1	IC 7490 is a a. Synchronous Counter b. Asynchronous Counter c. MOD 15 Counter d. MOD 8 Counter
2.	Loop is a _____ statement. a. Concurrent b. Sequential c. Assignment d. Functional
3	This is a universal shift register IC a. IC 74194 b. IC 74163 c. IC 7490 d. IC 7493
4.	What is the basic unit of behavioral description? a. Structure b. Sequence c. Process d. Dataflow
5	Those statement which are placed under _____ are concurrent. a. Process b. Function c. Architecture d. Procedure
6	A sequential Circuit with ten states will have a.10 Flipflops b.5 Flip Flops c.4 Flipflops d.0 Flipflops
7	This is not a logical operator in VHDL a. AND b. OR c. Multiplexer d. NOR
8	In which architecture component is declared a. Structural architecture b. Behavioural architecture c. Data flow architecture d. Process architecture
9	Which architecture is preferable for sequential circuit design a. Behavioural architecture b. Process architecture c. Structural architecture d. Data flow architecture

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10.	ASM chart represents a. Gates b. Multiplexers c. Synchronous sequential circuits d. PLA's
11.	Machine whose output does not depend on external input. a. Mealy b. Sequential asynchronous c. Asynchronous d. Moore
12	._____ is a synchronous 4 bit binary counter IC. a. IC 7490 b. IC 74163 c. IC 74194 d. IC 7492
13.	A decision box in an ASM chart does not a. Have exit paths b. Has only one exit Path c. Has two exit paths d Has one entry and one exit path
14.	IC 74169 is a. UP/DOWN counter IC b. UP counter IC c. Down counter IC d.BCD counter IC
15.	In mealy machine ,the output depends upon a. State b. Previous State c. State and Input d. Only Input
16	A for loop is initiated as given below, in total how many iterations will be there for the FOR loop? For i in 0 to 5 loop a.3 b.4 c.5 d.6
17	VHDL stands for a. VHSIC Hardware Description Language b. VHSIC Hardware Described Language c. VLSI Hardware Description Language d. VHSS Hardware Description Language
18	Which method is not a state reduction method

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	a. Implication Chart method b. Row elimination method c, Partition method d. Computer aided method
19.	PAL is__ a. Programmable AND array and fixed OR array b. Programmable OR array and fixed AND array c. Both (AND ,OR)are programmable d .Both are fixed
20.	FPGA stands for a. Field Programmable Gate Application b. Field Programmable Gate Array c. Field Programmable Gala Array d. FET Programmable Gate Array
21.	PROM is a. AND array is fixed and OR array is programmable b. Both AND and OR arrays are programmable c. OR array is fixed and AND array is programmable d. Both AND and OR arrays are fixed
22.	A ROM of size M*N bits can store a. N words of M bits each b. M words of N bits each c. M bits d. N bits
23	Identify this is not a predefined data type in VHDL a. Std_logic b. Std_logic_vector c. Bit d. Long float
24.	The signal assignment is considered as a _____ a. Concurrent statement b. Sequential statement c. Subprogram d. Package declaration statement
25.	An ASM chart consist of a. Only state boxes b. Only Decision boxes c. Only decision and conditional output boxes d. State decision and conditional output boxes