University of Mumbai

Examination 2020

Program: BE Electronics Engineering

Curriculum Scheme: Revised 2016 (CBCGS)

Examination: Second Year Semester III

Course Code: ELX303 Course Name: Digital Circuit Design

Time: 1 hour **Max. Marks: 50**

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Note:

1. All Questions are compulsory and carry equal marks.

2. Assume suitable data wherever necessary.

Q1.	Convert $(615)_8$ to the Hexa-decimal.
Option A:	18C
Option B:	18D
Option C:	195
Option D:	185
Q2.	One's complement of a binary number 1011 0011 is
Option A:	01001100
Option B:	01100101
Option C:	10010100
Option D:	01001101
Q3.	Which of the following single multiplexer is sufficient to implement the function f((a,b,c)=∑m(0,2,3,6)
Option A:	2:1 Multiplexer
Option B:	4:1 Multiplexer
Option C:	8:1 Multiplexer
Option D:	16:1 Multiplexer
Q4.	Which code is called non-weighted code ?
Option A:	Excess -3 code
Option B:	8421 Code
Option C:	Binary Code
Option D:	BCD code
Q5.	In Hamming code this expression will help you to find out no of parity bits.
Option A:	$2^P>=P+M+1$
Option B:	$2^P<=P+M+1$
Option C:	$2^P=P+M-1$
Option D:	$2^P<=P+M-1$

Q6.	How many gates are required to implement OR gate using only NAND gates?
Option A:	3
Option B:	2
Option C:	1
Option D:	4
Q7.	Half Subtractor is realized by using
Option A:	One X-OR Gate and one AND Gate
Option B:	One X-OR Gate and one OR Gate and one NOT Gate
Option C:	One X-OR Gate and one AND Gate and one NOT Gate
Option D:	One X-OR Gate and one OR Gate
Q8.	IC 74151 enable pin
Option A:	Active low
Option B:	Active High
Option C:	High Impedance
Option D:	+12v
Q9.	For even parity checker ,this Gate is used
Option A:	Ex-OR
Option B:	Ex-NOR
Option C:	NAND
Option D:	NOR
Q10.	IC 74138 is a
Option A:	Multiplexer
Option B:	Adder
Option C:	Comparator
Option D:	Decoder
Q11.	The code used for labelling cells of the K-map is
Option A:	Natural BCD
Option B:	Hexadecimal
Option C:	Gray
Option D:	Octal
Q12.	_____ is a graphical method of reduction of logic function.
Option A:	Boolean Algebra
Option B:	Logic Table
Option C:	Logic array
Option D:	K-map

Q13.	Convert $(125.62)_8$ to binary
Option A:	1010101.11011
Option B:	1111101.101
Option C:	1010101.11001
Option D:	1010101.01100010
Q14.	Figure of merit of IC family is
Option A:	Gate propagation delay
Option B:	Gate power Dissipation
Option C:	Speed power product
Option D:	fan out
Q15.	The fan in of a logic Gate is defined as the
Option A:	Number of inputs that the Gate is designed to handle
Option B:	Number of Outputs that the Gate is designed to handle
Option C:	Number of input /Outputs that the Gate is designed to handle
Option D:	Number of tristate that the Gate is designed to handle
Q16.	A TTL circuit act as a current sink
Option A:	Low state
Option B:	High State
Option C:	High Impedance state
Option D:	low impedance state
Q17.	When the flipflop is set ,it's output will be
Option A:	Q=0, Q=0
Option B:	Q=0, Q=1
Option C:	Q=1, Q=1
Option D:	Q=1, Q=1
Q18.	How many states a 6 bit ripple counter can have
Option A:	6
Option B:	12
Option C:	32
Option D:	64
Q19.	The minimum no of flipflop required a mod 12 Johnson counter is
Option A:	4
Option B:	6

Option C:	12
Option D:	24
Q20.	The circuit which changes from serial data to parallel data
Option A:	Counter
Option B:	Demultiplexer
Option C:	Multiplexer
Option D:	FlipFlop
Q21.	The characteristics equation of D ff
Option A:	Qn+1=D
Option B:	Qn+1=Qn
Option C:	Qn+1=1
Option D:	Qn+1=0
Q22.	1:8 Demultiplexer ,number of select lines
Option A:	2
Option B:	3
Option C:	4
Option D:	5
Q23.	Which is not a combinational circuit
Option A:	Multiplexer
Option B:	Counter
Option C:	Decoder
Option D:	Adder
Q24.	NOR Gate is equivalent to
Option A:	Bubbled AND gate
Option B:	Bubbled OR gate
Option C:	Bubbled NAND gate
Option D:	Bubbled NOT gate
Q25.	According to Boolean laws(A+AĀ)=?
Option A:	Ā
Option B:	A
Option C:	A Ā
Option D:	A+1

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