

SAMPLE PAPER

Examinations Commencing from 23rd December 2020 to 6th January 2021

Program: Electronics Engineering

Curriculum Scheme: Rev 2016

Examination: BE Semester VII

Course Code: ELX703 Course Name: Digital Signal Processing

Time: 2 hour

Max. Marks: 80

Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	One of the output values in the 4 point DFT of the sequence $x(n)=\{5,6,7,8\}$ is
Option A:	25
Option B:	29
Option C:	26
Option D:	30
2.	The energy of the sequence whose DFT is $\{6, -2+2j, -2, -2-2j\}$ is
Option A:	14
Option B:	16
Option C:	18
Option D:	20
3.	Compute DFT of the sequence $x(n)= [1,1,0,0]$
Option A:	$[2,1-j,1,1+j]$
Option B:	$[2,1-j,0,1+j]$
Option C:	$[2,1+j,0,1-j]$
Option D:	$[2,1+j,1,1-j]$
4.	If $N= 16$, the total number of complex multiplications and additions required respectively for computing N point DFT by radix-2 FFT are
Option A:	80 and 64
Option B:	64 and 80
Option C:	32 and 64
Option D:	24 and 12
5.	Number of complex additions and complex multiplications in DFT are:

Option A:	$N(N-1)$ and N^2
Option B:	N^2 and N
Option C:	$N \cdot \log(N)$ and $(N-1)$
Option D:	N and N^2
6.	In the impulse invariant transformation RHS of S plane is mapped to
Option A:	Inside the unit circle in the Z plane
Option B:	Outside the unit circle in the Z plane
Option C:	On to the unit circle in the Z plane
Option D:	RHS of the Z plane
7.	In Butterworth and Chebyshev transfer function, when N is even, the nature of poles are _____
Option A:	Complex and exist as conjugate pairs
Option B:	Complex but not conjugate pairs
Option C:	One pole is complex and other poles are real
Option D:	One pole is real and other poles are complex and conjugate
8.	The roots of an Nth order Chebyshev polynomial $C_n(x)$ occur in the interval
Option A:	$0 \leq x \leq 1$
Option B:	$-1 \leq x \leq 0$
Option C:	$-1 \leq x \leq 1$
Option D:	$-0.5 \leq x \leq 0.5$
9.	Find the digital transfer function $H(z)$ by using impulse invariant method for the analog transfer function $H(s) = 1/(s+2)$. Assume $T=0.5$ sec
Option A:	$H(z) = 1/(1 - e^{-1} z^{-1})$
Option B:	$H(z) = 1/(1 - e^{-1} z^{-1})$
Option C:	$H(z) = 1/(1 - e^{-1} z^{-1})$
Option D:	$H(z) = 1/(1 - e^{-2} z^{-1})$
10.	Linear FIR filter which is having even symmetry and even length is called _____
Option A:	Type 1
Option B:	Type 2
Option C:	Type 3
Option D:	Type 4
11.	For a digital bandstop filter with lower stop band edge frequency 100 Hz and upper stop band edge frequency 200 Hz and sampling frequency 1 kHz, what is the filter coefficient at $n=0$, ie $h(0)$ is _____

Option A:	0.2
Option B:	0.8
Option C:	0.4
Option D:	0.6
12.	What is the width of the main lobe of the frequency response of a rectangular window of length M ?
Option A:	π/M
Option B:	$2\pi/M$
Option C:	$4\pi/M$
Option D:	$8\pi/M$
13.	If an FIR filter has constant phase delay as well as constant group delay and N is odd then it is of type_____
Option A:	Type I
Option B:	Type II
Option C:	Type III
Option D:	Type IV
14.	The dynamic range in bits in image processing applications is of the order of ____
Option A:	10 bits
Option B:	20 bits
Option C:	30 bits
Option D:	70 bits
15.	How is the sensitivity of filter coefficient quantization for FIR filters?
Option A:	High
Option B:	Low
Option C:	Moderate
Option D:	Unpredictable
16.	A 3 stage decimator is used to reduce the sampling rate from 3072 kHz to 48 kHz. What is the overall decimation factor?
Option A:	64
Option B:	32
Option C:	128
Option D:	256
17.	Consider the discrete time sequence: $x(n) = \{1, 2, 3, 4\}$. Converting the sampling rate by a factor ($\frac{2}{3}$) will result in:
Option A:	$\{1, 0, 2, 0, 3, 0, 4, 0\}$

Option B:	{1, 0, 4}
Option C:	{1, 3}
Option D:	{1, 0, 0, 2, 0, 0, 3, 0, 0, 4, 0, 0}
18.	How many clock cycles are required when the MACD instruction is to be executed in a machine with Von Neumann Architecture?
Option A:	1
Option B:	2
Option C:	3
Option D:	4
19.	Which processor is having 2 multipliers?
Option A:	TMS320C10
Option B:	TMS320C6200
Option C:	DSP56300
Option D:	TMS320C50
20.	Which of the following DSP processor family has VLIW architecture?
Option A:	TMS3201X
Option B:	TMS3203X
Option C:	TMS3205X
Option D:	TMS3206X

Q2 .	Solve any TWO out of the given three questions. All the sub questions carry 10 marks each .Total marks for this question is 20 marks (20)
A	Find the DFT using decimation in frequency FFT algorithm. $x(n)=\{1,2,1,2,0,2,1,2\}$
B	Design a lowpass FIR filter with 11 coefficients for the following specifications . Passband edge frequency=0.25 kHz. Sampling frequency=1 kHz Use a)Hamming window. b)Hanning window
C	Given the transfer function $H(z)=H_1(z).H_2(z)$ Where $H_1(z)=1/(1-a_1z^{-1})$, $H_2(z)=1/(1-a_2z^{-1})$. Find the output roundoff noise power .Assume $a_1=0.5$ and $a_2=0.6$ and find the output roundoff noise power

Q3 .	Solve any TWO out of the given three questions. All the sub questions carry 10 marks each .Total marks for this question is 20 marks (20)
A	A highpass digital filter meeting the following specifications is required. Passband 2-4 kHz, Stopband=0-500 Hz Passband ripple=3 db Stopband attenuation =20db .Sampling frequency=8 kHz. Assume butterworth characteristics and use bilinear transformation.
B	Explain the process of decimation by a factor D with block diagrams.Draw the spectral diagrams.
C	Draw the block diagram of a 3 rd generation fixed point DSP processor and explain the features.