BE | Etrx | VII (Rev) 21/5/2015
MSD.

QP Code : 8466

(3 Hours) **[Total Marks : 100**

N.B : (1) Question No **1** is **compulsory.**
(2) Answer any **four** of the remaining questions.
(3) **All** questions carry **equal** marks.

1. (a) Explain different bus phase in SCSI. **5**
   (b) PCI bus is called 'Green Bus' Justify. **5**
   (c) Explain TAP port of Pentium Processor. **5**
   (d) Explain Methods of Invalidating cache line for Pentium Processor. **5**

2. (a) With respect to data cache of Pentium Processor explain cache line organization and Bank conflict in simultaneous data access. **10**
   (b) Explain with Neat diagram data bus steering while executing the following instruction. Assume 16-bit device interfaced to Pentium Processor. Indicate how many bus cycles are run for this operation. **10**
   MOV EAX, [4000012H]

3. (a) Explain IDE protocol for data read write command. **8**
   (b) Describe MESI protocol with suitable example **12**

4. (a) Explain how Interrupts are handled on PCI bus? Also explain how interrupts are routed on PCI bus. **10**
   (b) Describe PCI bus arbitration in detail. **10**

5. (a) Explain following terms of USB bus **10**
      (i) Host Controller and its function
      (ii) NAK and ACK Token
      (iii) Transaction Frame
   (b) Explain following signals in SCSI, **10**
   ATN, MSG, BSY, SEL, REQ, ACK

6. (a) Describe Branch prediction Logic in Pentium Processor. **10**
   (b) Explain split line Access with neat diagram. **10**

7. Write Short Notes on: **20**
   (a) Explain what is sector Interleave and its use in disk Drive?
   (b) Explain USB bus topology
   (c) PCI Write Cycle.

B.E. VII (R) (ETRX)
W/ Comm

21/5/15

Q.P. Code : 8460

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question **no. 1** is **compulsory**.
(2) Attempt **any four** questions from **remaining six** questions.
(3) Assume **suitable data** if **required**, stating them clearly.
(4) **Figures** to the **right** indicate **full marks**.

1. Answer any **four** of the following :- **20**
   (a) What is frequency reuse concept?
   (b) Explain umbrella cell approach in cellular systems.
   (c) Define the following terms :
      (i) Traffic intensity.
      (ii) Grade of Service.
      (iii) Blocked call
      (iv) Set up time.
      (v) Request time.
   (d) Explain pulse shaping in OFDM
   (e) Sketch and explain GSM frame structure.

2. (a) Co-channel interference determines the capacity of a cellular system. Explain. **5**
   (b) Assume a system of 32 cells with a cell radius of 1.6 km, total frequency bandwidth that supports 336 traffic channel and a reuse factor of N = 7. **10**
      (i) What is the geographic area covered?
      (ii) How many channels are there per cell?
      (iii) What is the total number of concurrent calls that can be handled?
      (iv) Repeat the above calculations for a cell of radius 0.8 km and 128 cells. Comment on your results.
   (c) Explain Cell dragging. **5**

3. (a) Explain how a multicarrier system like of OFDM helps to reduce ISI in a fading channel. **6**
   (b) Sketch OFDM system block diagram and explain. **10**
   (c) In an OFDM system, if a total of 52 subcarriers, spaced at 312.5 KHZ are defined, find the total occupied bandwidth excluding the secondary lobes. **4**

[TURN OVER

4.	(a)	CDMA is effectively on FDMA/CDMA/FDD system. Explain.	4
	(b)	Explain the advantage of spreading the spectrum in CDMA. Explain Direct Square Spread Spectrum with transmitter and receiver block diagram.	10
	(c)	List and briefly explain logical channels of CDMA IS-95.	6
5.	(a)	With a suitable sketch, explain GSM architecture.	8
	(b)	Explain authentication, cipher key generation and encryption in GSM.	8
	(c)	List and explain the functions of common control channels in GSM.	4
6.	(a)	Explain CDMA 2000 layered architecture. Discuss MAC and LAC sublayers.	10
	(b)	Explain signal processing in GSM.	10
7.		Write short notes on any **four** :	20
		(a) RAKE receiver	
		(b) Bluetooth	
		(c) Erlang B and Erlang C systems	
		(d) Zigbee	
		(e) GPRS.	

B.E. ETRX VII (R)

DIPD

21/5/15

QP Code : 8469

Duration 3 Hours **Maximum marks 100**

Instructions :

1. Question No.1 is compulsory.
2. Out of the remaining questions attempt any four.
3. Figures in the bracket indicate maximum marks.

Q 1. Answer the following:

a) What do you mean by zero memory operations? [05]

b) Differentiate between 8 connectivity and m connectivity. [05]

c) What is truncated Huffman code? [05]

d) Justify the statement: " Laplacian filter is a high pass filter." [05]

Q 2.

a) Explain the following enhancement operations and draw the graph of transformation function: [10]

i) Dynamic range compression ii) Gray level slicing

b) Perform histogram equalization on the following image histogram and plot original and equalized histograms. [10]

Gray Level	0	1	2	3	4	5	6	7
Number of pixels	550	300	0	0	0	200	325	225

Q 3.

a) Explain in detail the types of data redundancies seen in digital images [10]

b) Explain the method of edge linking using Hough Transform. [10]

Q 4.

a) Calculate the 2DDFT and Hadamard transform of the image segment shown below using matrix multiplication method. [08]

$$f(x,y) = \begin{matrix} 0\,0\,1\,4 \\ 3\,1\,1\,4 \\ 1\,0\,1\,0 \\ 0\,2\,0\,2 \end{matrix}$$

b) Explain the importance of kernel separability property of 2DDFT in implementing 2DFFT. [06]

c) Differentiate between spatial and tonal resolution. [06]

Q 5.

a) Explain why it is difficult to threshold images with poor illumination. [10]

b) With the help of a neat block diagram, explain the working of a homomorphic filter. [10]

Q 6.

a) What are Fourier Descriptors? Explain how a two dimensional boundary is represented using Fourier Descriptors. [10]

b) Explain how Huffman code removes coding redundancy. [10]

Q 7. Write short notes on any **four** of the following: [20]

a) Moments

b) Wavelet transform

c) Digital water marking

d) Biometric authentication

e) Motion based segmentation

RJ-Con. 10025-15.

BE/ETRX/VII (Rev.)
Filter Design

15/5/2015.

Q.P. Code : 8395

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) **Assume** suitable **data** if necessary with proper justification.

1. Answer the following : **20**
   (a) Explain design procedure of elliptic filter.
   (b) Differentiate IIR and FIR filter.
   (c) Explain why impulse invariance technique is not suitable for the design of high frequency filters.
   (d) Explain the MMSE criterion.

2. (a) Write design steps of FIR filter using Kaiser window. **10**
   (b) Explain the concept and applications of Weiner filter. **10**

3. Design digital Chebyshev filter for the following specifications. **20**

   $0.91 \leq |H_d(e^{jw})| \leq 1$ for $w \leq 1500$ rad / sec

   $|H_d(e^{jw})| \leq 0.002$ for $w \leq 4000$ rad / sec

   Assume sampling frequency of 10KHz. Use Bilinear transformation technique for the design.

4. (a) Design digital FIR filter for the following specifications **12**

   $|H_d(e^{jw})| = 4e^{-j4w}$ for $|w| \leq 0.5\pi$

   $= 0$ otherwise

   Use Hamming window for the design.
   (b) Write a short note on primary resonator block. **8**

5. (a) Apply unpluse invariance technique to convert $H(s) = \frac{s+3}{(s+4)(s+10)}$ to $H(z)$ **10**

   Assume $T = 0.1$ sec.
   (b) Describe Leapfrog realization technique in detail. **10**

6. (a) Write a short note on RLS algorithm. **10**

   (b) Explain design steps of FIR filter using frequency sampling method. Give merits and demerits over window technique. **10**

7. Write short notes on. **(any TWO)** **20**

   (a) Switched capacitor filter

   (b) LMS algorithm

   (c) Matched Z-Transform

   (d) Higher-order filters

B.E. Sem. VII – ETRX – Rev. – 27/05/2015
Power Electronics & Drives

QP Code : 8528

(3 Hours) **[Total Marks :100]**

N.B. : (1) Questions No. **1** is **compulsory.**
(2) Solve **any four** questions out of remaining **six** questions.
(3) Figures to the **right** indicate **full** marks.
(4) Assume **suitable** data **if** required.

1. Answer the following :- **20**
   (a) List the advantages of dc chopper drives over line commutated converter controlled dc drives.
   (b) Explain how semiconverter provides better power factor compared to full converter when both are working as rectifier with RL load.
   (c) What are advantages of flyback converter compared to forward converter?
   (d) Compare between current source and voltages source inverters.

2. (a) Draw and explain the operation of speed control of a DC series motor fed by a single phase semiconverter for the continuous motor current. Draw also the associated voltage and current waveforms. **10**
   (b) A 220 V, 1500 rpm, 10 A separately excited dc motor has an armature resistance of 1 ohm. It is fed from a single phase fully controlled bridge rectifier with an ac source voltage of 230, 50 HZ. Assuming continuous load current, compute :- **10**
      (i) Motor speed at firing angle of 30^0 and torque of 5 NM.
      (ii) Developed torque at firing angle of 45^0 and speed of 1000 rpm.

3. (a) Explain the operation of dual converter with circulating current. What are the advantages and disadvantages of the same? **10**
   (b) With neat circuit diagram explain the working of load commutated chopper with relevant voltage and current waveforms. Show voltage variation across each pair of SCRs as a function of time. **10**

4. (a) Explain the working of McMurry bridge inverter using circuit diagram and appropriate waveforms. **10**
   (b) Explain the operation of Induction Motor for two different cases when fed by current source inverter. **10**
      (i) Operation at and below rated frequency
      (ii) Operation above rated frequency

[TURN OVER]

5. (a) Discuss the stator voltage control scheme of induction motor, Also draw and explain the speed torque curves. 10
   (b) Explain the working of parallel inverter employing feedback diodes. Draw the voltage and current waveforms. What care should be taken to avoid commutation failure. 10

6. (a) Using block diagrams discuss different configurations of UPS 10
   (b) Draw and explain the operation of flyback converter with relevant waveforms. 10

7. Write short notes on :- 20
   (a) Effect of source inductance on performance of converter.
   (b) Harmonic reduction in inverters
   (c) Selection of battery in UPS.

B.E. Sem VII (R) (O) ETRX. 02/6/2015

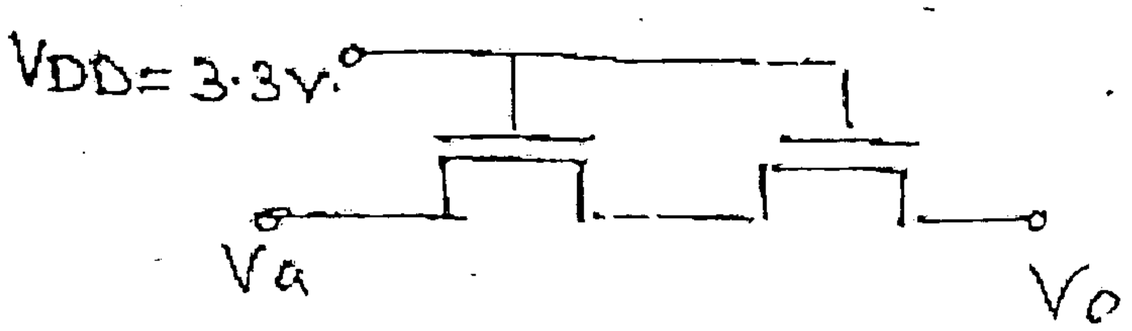
VLSI Design

QP Code : 8599

(3 Hours) [Total Marks : 100

N.B: (1) Question No.1 is **Compulsory**.
(2) Attempt any **Four** out of remaining **six** questions.
(3) Assume suitable **data** wherever **necessary**

1. Attempt any **four** : 20
   (a) Compare ion implantation and diffusion.
   (b) Draw VTC of three CMOS inverter with $K_R = 1$, $K_R < 1$ & $K_R > 1$.
   (c) Two n-MOS transistors (M1 & M2) connected in series shown in fig find output voltage for
   i) Va = 2.7 V, ii) Va = 3V.
   $V_{TH} = 0.7V$



   (d) Explain MOSFET works as a capacitor. 10

2. (a) Explain operation of CMOS inverter with clearly mentioning the five cases given below. 10
   (i) $V_{in} < V_{TO,n}$
   (ii) $V_{in} = V_{IL}$
   (iii) $V_{in} = V_{IH}$
   (iv) $V_{in} > V_{DD} + V_{TO,P}$
   (v) $V_{in} = V_{TH}$

   (b) Draw the p-well CMOS inverter and explain the latch up effect in it. What are remedies to avoid latch up problem. 10

3. (a) Calculate threshold voltage V_{TO} at $V_{SB} = 0$ for a polysilicon gate n-channel MOS transistor with following parameters. 10
   $N_A = 10^{16} cm^{-3}$, $N_D = 2 \times 20^{20} cm^{-3}$
   $t_{ox} = 200$ °A $N_{SS} = 5 \times 10^{11} cm^{-2}$
   (b) Write a verilog code for 4 × 4 barrel shifter. 10

4. (a) Draw a circuit diagram, stick diagram and layout for following equation 10

$$Y = \overline{A \cdot B \cdot C}$$

Use CMOS technology.

(b) Consider a CMOS inverter circuit with the following parameters 10

$V_{DD} = 3.3V$ $V_{TO,n} = 0.6V$ $V_{TO,p} = -0.7V$
$\mu_n C_{ox} = 60\mu A/V^2, (W/L)_n = 8$
$\mu_p C_{ox} = 20\ \mu A/V^2, (W/L)_p = 12$

Calculate the noise margin.

5. (a) Describe the hot electron and short channel effect in MOS device. Also explain their effect on MOS characteristic. 10

(b) Explain necessity of design rules ? Explain λ based design rules in detail. 10

6. (a) Define scaling. Explain constant voltage and constant field scaling in detail. 10

(b) Explain the method to design 4:1 MUX using NMOS pass transistor logic. Draw complete stick diagram. 10

7. Write a short notes on (any **three**) : 20

(i) MOS CV characteristics
(ii) VLSI design flow
(iii) Semicustom and full custom design
(iv) Transistor sizing.

BE Sem. VII | Electronics | Comm. Network
8 May 2015
8 June 2015

Q.P. Code : 8717

(3 Hours) **[Total Marks : 100**

N.B: Compulsory, answer any four from remaining six questions.

1 Answer the following briefly: **20**

(i) Distinguish between Logical Addressing. Physical Addressing and Port addressing. Give an example for each type . Also name the layer at which each of them operate.

(ii) What are transmission impairments ? Explain each briefly. Which transmission medium is better as a communication channel and why?

(iii) Explain the working of TSI Switch.

(iv) Compare TCP and UDP.

(v) What is meant by data transparency? How is it implemented in HDLC ? Give an example.

2. (a) Explain the need for layered architecture. Explain TCP/IP, mentioning the functions of each layer . Also mention the Protocols for each layer. **10**

(b) Explain the functions of each of these interconnecting devices: Hubs, Repeaters, Switches, Bridges, Routers and Gateways **10**

3 (a) Consider that Primary station A, is intending to set up communication link in normal response mode with two secondary Stations, B and C. Which frames are exchanged between Primary and Secondary stations for the following situations? Show with frame flow diagram, the following sequence : **10**

(i) Primary A wants to set up a normal response mode with secondary stations B and C and both stations B,C send an positive Acknowledgement frame to A

(ii) Station A wants to know whether B and C have some data to send to Primary and in response, B sends 2 data frames, while C indicates that it has no data to send.

(iii) Primary station sends acknowledgement to B for the data received.

(iv) Primary sends 'Select' command to Band 'C' to check whether any station is ready to receive the data. B indicates that it is Busy and not ready , while C indicates it is ready to receive the data.

(v) Primary sends 3 data frames to C and C sends positive acknowledgement to A.

(b) What is meant by error control? Show ,with flow diagrams, how error control is implemented in each ARQ technique for the following situations: 10

(i) lost or damaged frames,

(ii) delayed acknowledgments and

(iii) lost or damaged acknowledgements

4. (a) What is meant by 'blocking' in circuit switching networks? Bring out the advantages of multi stage space division switching over single stage switching. 10

(i) Sketch a 3-stage Space division switch with N = 15, group size of n = 5, K=2, what is the condition required to make it non-blocking? (ii) For the same specifications sketch three-stage TST switch using TSI modules. 10

(b) Explain ADSL with respect to Channel configuration and modulation technique. Compare the different DSL technologies.

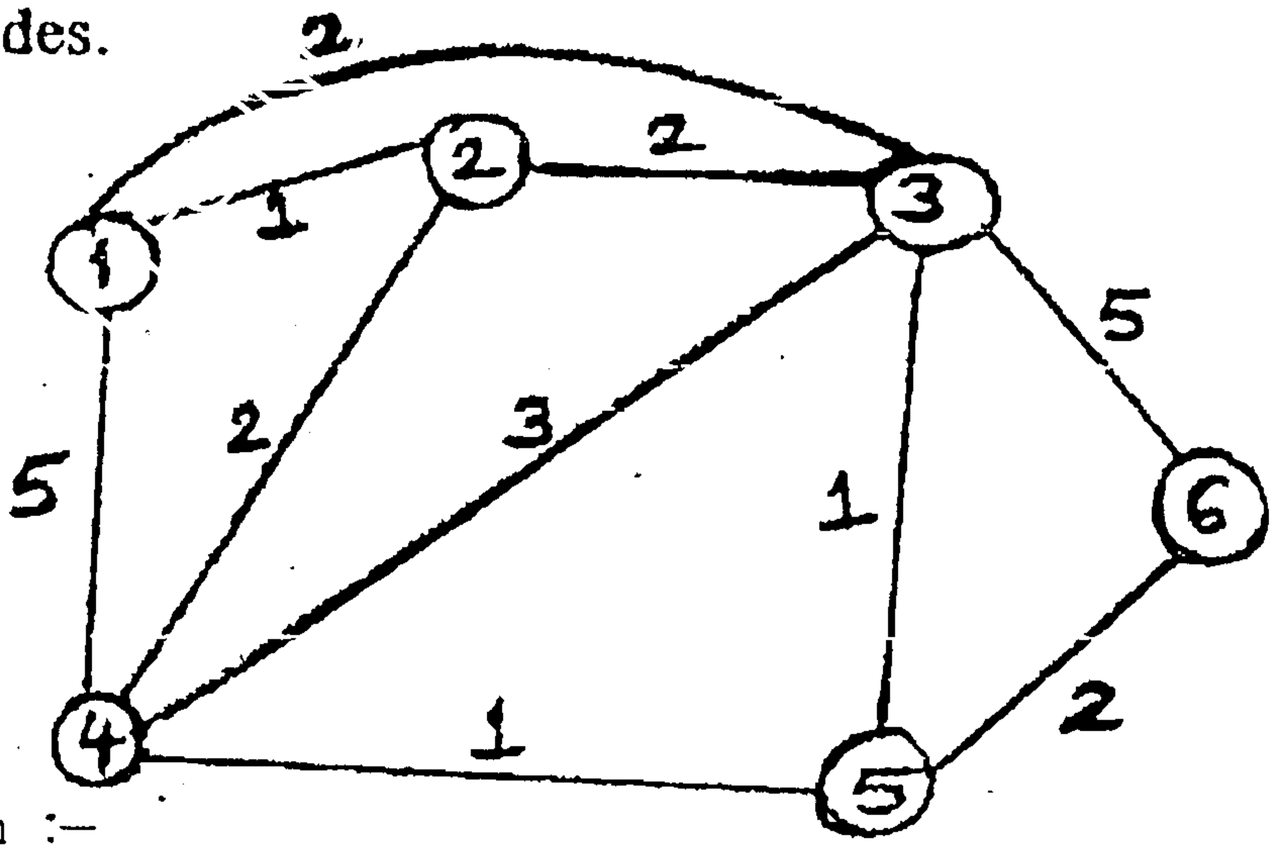
5. (a) Explain LAN Protocol architecture with reference to IEEE 802. Sketch the frame format of MAC Sub-layer and explain the functions of each field. 10

(b) What is the difference between Congestion Control and Flow control? Explain congestion control methods. 10

6. (a) Compare Circuit switching, Datagram switching and Virtual circuit Packet switching. 10

(b) Apply Dijkstra's algorithm to given network to find the least cost path from node 4 to all other nodes (state the steps in the algorithm). 10

nodes.



on :—

7. (a) Write short notes on (any four) : 20

(a) ISDN (b) Piggybacking with an example (c) Berkeley API

(d) SONET / SDH (e) LAN topologies.