University of Mumbai
Examination 2021
Program: **Electronics Engineering**
Curriculum Scheme: Rev 2016
Examination: ME Semester I(CBCGS)
Course Code: ELXDLO1011 **and Course Name:** Advanced Processor Architecture-I

Time: 2 hour Max. Marks: 80

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	80386 operates in how many modes ?
Option A:	3
Option B:	2
Option C:	1
Option D:	4
Q2.	How many segment registers in 80386 ?
Option A:	2
Option B:	4
Option C:	6
Option D:	7
Q3.	In CRO MP bit represents ?
Option A:	Math present
Option B:	Maximum Parity
Option C:	Minimum Parity
Option D:	Math parity
Q4.	For address translation mechanism of 386 in real mode
Option A:	Segment base address + limit = 16 bit physical address
Option B:	Segment base address + limit = 20 bit physical address
Option C:	Segment base address + limit = 32 bit physical address
Option D:	Segment base address + offset = 32 bit physical address
Q5.	If base address of global descriptor table is 00011000H and the selector is 2108H. What is the address range of TSS descriptor ?
Option A:	00013101 H to 0001310F H
Option B:	00013102 H to 0001310F H
Option C:	00013108 H to 0001310F H
Option D:	00013105 H to 0001310F H
Q6.	RISC stands for
Option A:	Risk Instruction Set Computers
Option B:	Rapid Instruction set Computers
Option C:	Raw Instruction set Computers

Option D:	Reduced Instruction Set Computers
Q7.	SIMD is known as
Option A:	Single Instruction
Option B:	Multiple Stream
Option C:	Single Instruction Mutiple Data Stream
Option D:	Multiple Instruction Single Data Stream
Q8.	Pentium processor is a ---------- bit processor
Option A:	64 bit
Option B:	32 bit
Option C:	16 bit
Option D:	8 bit
Q9.	Which architecture makes pentium processor faster
Option A:	superscalar
Option B:	harvard
Option C:	VonNeuman
Option D:	pipelined
Q10.	BTC stands for
Option A:	Branch Cache
Option B:	Branch Target Cache
Option C:	Bi Target Cache
Option D:	Branch Trace Cache
Q11.	How many stage pipeline logic pentium supports?
Option A:	1 stage
Option B:	2 stage
Option C:	3 stage
Option D:	5 stage
Q12.	Cache Hits/Total memory requests x 100 is defined as
Option A:	miss rate
Option B:	cache hit
Option C:	cache rate
Option D:	hit rate
Q13.	Mention principles of localities of cache memory in pentium?
Option A:	Temporary and permanent
Option B:	Temporal and permanent
Option C:	Temporal and Spatial
Option D:	Temporary and spatial
Q14.	Two types of cache architectural designs
Option A:	Look through and Look Aside

Option B:	Look back and Look aside
Option C:	look through and look back
Option D:	look back and look into
Q15.	Which write policy is easy to implement but tedious
Option A:	write through policy
Option B:	write back policy
Option C:	buffered write back policy
Option D:	buffered write through policy
Q16.	Write policy which creates cache coherency issues
Option A:	Write through policy
Option B:	write back policy
Option C:	buffered write back policy
Option D:	buffered write through policy
Q17.	Unit which handles floating numbers in pentium?
Option A:	Integer unit
Option B:	Floating point unit
Option C:	arithmatic unit
Option D:	logic unit
Q18.	cache coherency is maintained in pentium processor via this operation
Option A:	cache line fill
Option B:	Snooping and snarfing
Option C:	line fill
Option D:	LRU algorithm
Q19.	Pentium processor has -------, ------- caches
Option A:	L1,L2
Option B:	L1, L3
Option C:	L1,L4
Option D:	L2,L4
Q20.	Internal cache memory of pentium follows ----------Architecture
Option A:	Von Neuman
Option B:	Superscale
Option C:	Harvard
Option D:	Neuman

Q2 (20 Marks Each)	**Solve any Two out of Three 10 marks each**
A	Explain architecture and software model of 80386 with neat diagram?
B	Explain in order and out of order execution methods with suitable examples?
C	Write short notes: a) SMP and CMP b) Laws of Parallelism c) VLIW processors d) Protection mechanism of 80386

Q3. (20 Marks Each)	Solve any Two out of Three 10 marks each
A	Explain cache structure and split line access with respect to Pentium processors?
B	With neat diagram state the features, types and advantages of Multiprocessor Organization?
C	Compare in detail Cluster and NUMA multiprocessor organizations?