University of Mumbai

Program: **Computer Engineering**
Curriculum Scheme: Rev2019
Examination: Second Year Semester: III
Course Code: CSC304 Course Name: Digital Logic and Computer Architecture

Time: 2.5 hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Structural hazard arises due to
Option A:	Data conflict
Option B:	Resource conflict
Option C:	Branch conflict
Option D:	Address conflict
2.	What is the value of n in Booth's multiplication of 101* 1001?
Option A:	2
Option B:	3
Option C:	4
Option D:	0
3.	The addressing mode used in an instruction of the form ADD AX , 07h is
Option A:	Direct
Option B:	Indirect
Option C:	Immediate
Option D:	Absolute
4.	In the memory hierarchy, as we go down the pyramid,
Option A:	Cost per bit decreases, Capacity increases, Access Time increases
Option B:	Cost per bit increases, Capacity decreases, Access Time decreases
Option C:	Cost per bit increases, Capacity increases, Access Time decreases
Option D:	Cost per bit decreases, Capacity decreases, Access Time decreases
5.	In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____.
Option A:	D flip-flop
Option B:	S-R flip-flop
Option C:	T flip-flop
Option D:	S-K flip-flop

6.	Select true statement from the following.
Option A:	USB is a parallel mode of transmission of data and this enables for the fast speeds of data transfers.
Option B:	In USB the devices can communicate with each other.
Option C:	The type/s of packets sent by the USB is/are Data.
Option D:	When the USB is connected to a system, its root hub is connected to the Processor BUS.
7.	Which of the following statements is false?
Option A:	Diagonal micro-instructions encoding requires multiple decoders.
Option B:	In vertical micro-instructions encoding, more than one control signals cannot be activated at a time.
Option C:	Horizontal micro-instructions encoding has a lower cost of implementation.
Option D:	On one end of a spectrum, a *vertical* microinstruction is highly encoded and may look like a simple macroinstruction containing a single opcode field and one or two operand specifiers.
8.	A second factor in locality of reference is the presence of loops in programs. Instructions in a loop, even when they are far apart in spatial terms, are executed repeatedly, resulting in a high frequency of reference to their addresses. This characteristic is referred to as _____.
Option A:	Spatial locality.
Option B:	temporal locality
Option C:	branch locality.
Option D:	Equidistant locality
9.	In parallelization, if P is the proportion of a system or program that can be made parallel, and 1-P is the proportion that remains serial, then the maximum speed up that can be achieved using N number of processors is 1/((1P)+(P/N). This law is called _____
Option A:	Newton's law
Option B:	Ohms law
Option C:	Amdahl's law
Option D:	Flynn's law
10.	Arbitration does not fail when_____
Option A:	devices on the bus have logic errors
Option B:	manufacturing defects
Option C:	are driven beyond their design speeds
Option D:	more devices compete for the control of the bus

Q2. (20 Marks)	Solve any Four out of Six. 5 marks each
A	Explain Booth's Algorithm. Perform multiplication of (-12 * 5) using booths algorithm.
B	Explain Von Neumann model. What is the role of different registers like IR, PC, MAR, MBR in Von Neumann model.
C	What is flip flop? Write truth table of SR, JK, D, T flip flop.
D	Explain instruction cycle with neat diagram.
E	What is bus arbitration? Explain types of bus arbitration.
F	Explain various pipeline hazards.

Q3. (20 Marks)	Solve any Two Questions out of Three 10 marks each
A	Differentiate between hardwired and microprogrammed control unit and Explain Wilke's Microprogrammed control unit with neat diagram.
B	Consider a cache memory of 16 words. Each block consists of 4 words. Size of the main memory is 256 bytes. Draw associative mapping and Calculate TAG & WORD size.
C	Explain Flynn's classification.

Q4. (20 Marks)	Solve any Two Questions out of Three 10 marks each
A	Draw the flowchart of Restoring Division Algorithm & perform 10 /3 using this Algorithm.
B	What is meaning of delayed branch and branch prediction? Write a difference between them.
C	What are the features of cache memory design?