Program: BE Computer Engineering

Curriculum Scheme: Revised 2016

Examination: Second Year Semester IV

Course Code: CSC403 and Course Name: Computer Organization And Architecture

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	The bit pattern 0 10000000 10010111010010111100011 when interpreted as a IEEE 754 single precision number, represents ------- in the decimal number system.
Option A:	3.182
Option B:	-3.182
Option C:	30.182
Option D:	300.182
Q2.	The IEEE 754 double precision floating point format the value of the bias is ----.
Option A:	511
Option B:	127
Option C:	1023
Option D:	255
Q3.	Microprogramming is a concept associated with designing of ------.
Option A:	Arithmetic Logic Unit
Option B:	Bus Interface Unit
Option C:	Control Unit
Option D:	Memory Management Unit
Q4.	Which of the following statements is FALSE about the control unit.
Option A:	Hardwired control units are faster than microprogrammed control units.
Option B:	Hardwired control units have much more complex design than microprogrammed control units.
Option C:	Hardwired control units are very flexible when it comes to making changes in their design.
Option D:	Microprogrammed control units are much more flexible when it comes to making

	changes in the design.
Q5.	Which of the following statements is TRUE?
Option A:	RISC machines use hardwired control units.
Option B:	CISC machines use hardwired control units.
Option C:	RISC machines have a few number of CPU registers

Option D:	RISC machines have instructions which have non-uniform length.
Q6.	Which of the following statements is TRUE about microprogramming?
Option A:	Vertical microprograms take more time to generate control signals.
Option B:	Horizontal microprograms take more time to generate control signals.
Option C:	Vertical microprogramming reduces the complexity of the microinstructions.
Option D:	Horizontal microprogramming reduces the length of the microinstructions.
Q7.	The register, IR is meant for ….
Option A:	Holding operands being used by the instructions.
Option B:	Holding the instruction being interpreted.
Option C:	Holding the instruction that is being fetched.
Option D:	Holding the address of the instruction that is being fetched.
Q8.	The register PC ------
Option A:	holds the address of the next instruction to be fetched.
Option B:	holds the next instruction to be fetched.
Option C:	holds the operands that are being fetched.
Option D:	holds the result of the last instruction.
Q9.	What will be the contents of Accumulator, Multiplier and Q-1 registers if the multiplication of -52 and 59 is done using Booth's algorithm.
Option A:	111110101 00000100 0
Option B:	111110100 00000100 0
Option C:	011110100 00000100 1
Option D:	111110100 11000100 0
Q10.	Stored program concept was given by ----.
Option A:	John Von Neumann
Option B:	Alan Turing
Option C:	Charls Babbage
Option D:	Edsger W. Dijkstra

Q11.	Structural hazard arises due to_____
Option A:	Data conflict
Option B:	Resource conflict
Option C:	Branch conflict
Option D:	Address conflict
Q12.	Which operation is performed in booth's algorithm.
Option A:	Arithmetic left shift
Option B:	Logical left shift
Option C:	Arithmetic right shift
Option D:	Logical right shift
Q13.	Result of the division (7/3) by using restoring division algorithm is
Option A:	M = 0111, Q = 0001, A = 0010
Option B:	M = 0011, Q = 0010, A = 0001
Option C:	M = 0111, Q = 0010, A = 0001
Option D:	M = 1111, Q = 0010, A = 0001
Q14.	The addressing mode used in an instruction of the form ADD AX , 07h is _____
Option A:	Direct
Option B:	Indirect
Option C:	Immediate
Option D:	Absolute
Q15.	In the memory hierarchy, as we go down the pyramid,
Option A:	Cost per bit decreases, Capacity increases, Access Time increases
Option B:	Cost per bit increases, Capacity decreases, Access Time decreases
Option C:	Cost per bit increases, Capacity increases, Access Time decreases
Option D:	Cost per bit decreases, Capacity decreases, Access Time decreases
Q16.	Spatial locality refers to_____
Option A:	the tendency of a program to access data locations sequentially
Option B:	the tendency of a program to access data locations randomly
Option C:	the tendency for a processor to access memory locations that have been used recently

Option D:	the tendency for a processor to access memory locations that have never been used
Q17.	The maximum amount of information that can be transferred to or from the memory per unit time is called
Option A:	Frequency
Option B:	Bandwidth
Option C:	Access time
Option D:	Cycle time
Q18.	The instruction, MOV AX, [3500H] is an example of
Option A:	immediate addressing mode
Option B:	direct addressing mode
Option C:	indirect addressing mode
Option D:	register addressing mode
Q19.	Consider a direct mapped cache of size 64 KB with block size 16 bytes. The CPU generates 28-bit addresses. The number of bits needed for cache indexing are respectively are:
Option A:	13
Option B:	11
Option C:	10
Option D:	12
Q20.	The method of accessing the I/O devices by repeatedly checking the status flags is
Option A:	Program-controlled I/O
Option B:	Memory-mapped I/O
Option C:	I/O mapped
Option D:	DMA
Q21.	The DMA transfer is initiated by _____
Option A:	Processor
Option B:	The process being executed
Option C:	I/O devices
Option D:	OS
Q22.	A word whose individual bits represent a control signal is _____
Option A:	Command word

Option B:	Control word
Option C:	Co-ordination word
Option D:	Generation word
Q23.	Which of the following is not the form of registers?
Option A:	Accumulator
Option B:	General purpose register
Option C:	Special purpose register
Option D:	Cache
Q24.	Which of the memory has highest speed?
Option A:	internal memory
Option B:	cache memory
Option C:	main memory
Option D:	secondary memory
Q25.	"loacality of reference" is related to which memory?
Option A:	Cache Memory
Option B:	Primary Memory
Option C:	Internal Registers
Option D:	Hard Disks