University of Mumbai

Examination 2020 under cluster (Lead College:)

Examinations Commencing from 7th January 2021 to 20th January 2021

Program: **Computer Engineering**

Curriculum Scheme: Rev2016

Examination: TE Semester V

Course Code: CSC501 and Course Name: Microprocessor

Time: 2 hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	What is the size of offset address in 8086 microprocessor?
Option A:	8 bit
Option B:	20 bit
Option C:	16 bit
Option D:	12 bit
2.	Which of the following is not a machine control flag?
Option A:	Interrupt flag
Option B:	Direction flag
Option C:	Trap flag
Option D:	Overflow flag
3.	What is size of segments of memory in 8086 microprocessor?
Option A:	1 KB
Option B:	64 KB
Option C:	1 MB
Option D:	Variable
4.	Which segment registers and offset registers combinations are true for 8086 processors?
Option A:	CS-IP; DS-SI; ES-DI; SS-SP
Option B:	CS-IP; DS-SI; ES-EI; SS-BP
Option C:	CS-SP; ES-SI; DS-DI; SS-BP
Option D:	CS-IP; DS-DI; ES-SI; SS-BP
5.	The memory location accessed by 8086 processor after reset condition is
Option A:	FFFFE h
Option B:	FFFFF h
Option C:	FFFF0 h
Option D:	00000 h
6.	Which instruction cannot force the 8086 processor out of ‘halt’ state?
Option A:	Interrupt request
Option B:	Reset
Option C:	both interrupt request and reset
Option D:	Hold

7.	Which one of the following chip is used to display lights at a particular port?
Option A:	8255(PPI)
Option B:	8288(Bus controller)
Option C:	8284(Clock generator)
Option D:	8087(Math co-processor)
8.	If the size of the segment is 64 kb, what will be the starting and ending offset addresses for it.
Option A:	0000H to 7FFFH
Option B:	0000H to FFFFH
Option C:	8000H to FFFFH
Option D:	00000H to FFFFFH
9.	Choose the appropriate term for the operation given below Memory to memory transfer without CPU intervention.
Option A:	Direct memory access
Option B:	Programmable peripheral interface
Option C:	Maximum mode
Option D:	Pipelining
10.	"In 8253 PIT, the three counters available are independent of each other in operation, but they are ---------- to each other in organization."
Option A:	Similar
Option B:	Opposite
Option C:	Identical
Option D:	Common

11.	For the following code, select what would be the contents of register CX and DX at end.
	MOV DX,0AH
	MOV CX,10H
	XCHG CX,DX
	ADD DX,02H

Option A:	CX=10H, DX=0AH
Option B:	CX=0AH, DX=12H
Option C:	CX=08H, DX=10H
Option D:	CX=12H, DX=08H
12.	MOV CX,0004H REPNE CMPSB The above set of instruction will repeat till
Option A:	Repeat instruction until CX=4 or zero flag ZF≠1.
Option B:	Repeat instruction until CX=0 or zero flag ZF=1
Option C:	Repeat instruction until CX=0 or zero flag ZF≠1
Option D:	None of above
13.	If CS = 2000H, IP = 0003H for the instruction: JZ 0AH, what would be the jump location address, if ZF=1.
Option A:	2000DH
Option B:	200DH

Option C:	200A3H
Option D:	20003H
14.	Which of the following instructions are incorrect?
Option A:	ADD CX,[000AH]
Option B:	SUB BL,AX
Option C:	MUL BX
Option D:	DIV BX,AX
15.	Number of debug registers available in 80386 are
Option A:	2
Option B:	4
Option C:	8
Option D:	16
16.	Paging unit is enabled in which one of the following mode of 80386?
Option A:	Virtual mode
Option B:	Real mode
Option C:	Protected mode
Option D:	Max mode
17.	Four level protection mechanism in 80386 is provided by which of the following unit?
Option A:	Central processing unit
Option B:	Bus interface unit
Option C:	Execution unit
Option D:	Segmentation unit
18.	Which of the following is not the feature of Pentium processor?
Option A:	U and V pipeline
Option B:	Two 8KB cache
Option C:	20-bit address bus
Option D:	On chip, memory management unit
19.	In Pentium pipelining, D1 stage does which of the following function.
Option A:	pairability check, branch prediction
Option B:	operand address calculation, protection/privilege check
Option C:	Instruction prefetch
Option D:	Calculates results in ALU
20.	MESI protocol requires Pentium to monitor all accesses to main memory in a multiprocessor system, this is called
Option A:	Control accessing
Option B:	Bus snooping
Option C:	Data binding
Option D:	Instruction Decoding

Descriptive Section

Q2 **(20 Marks)**	**Solve any Four out of Six** **5 marks each**
A	Explain the need of segmentation.
B	Explain 8086 interrupt execution procedure.
C	Write a short note on mixed language programming.
D	Explain mode-2 of 8255.
E	Explain Virtual mode of 80386DX.
F	How does an Integer Pipeline of Pentium processor works?

Q3. **(20 Marks)**	**Solve any Two Questions out of Three** **10 marks each**
A	Write Assembly Language Program for 8086 to reverse a string of 10 characters.
B	Explain any five operating modes of 8259 with diagram.
C	Design a 8086 system with the following specifications 1. 8086 working at 10 Mhz in minimum mode 2. 32 KB EPROM using 16 KB devices