University of Mumbai

Program: **Computer Engineering**
Curriculum Scheme: Rev2019
Examination: Second Year Semester: III
Course Code: CSC304   Course Name: Digital Logic and Computer Architecture

Time: 2 hour   Max. Marks: 80

==

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	The value of the bias in IEEE 754 double precision floating point format is ----.
Option A:	511
Option B:	127
Option C:	1023
Option D:	255
2.	The register PC ------
Option A:	holds the address of the next instruction to be fetched.
Option B:	holds the next instruction to be fetched.
Option C:	holds the operands that are being fetched.
Option D:	holds the result of the last instruction.
3.	Stored program concept was given by ----.
Option A:	John Von Neumann
Option B:	Alan Turing
Option C:	Charls Babbage
Option D:	Edsger W. Dijkstra
4.	Structural hazard arises due to
Option A:	Data conflict
Option B:	Resource conflict
Option C:	Branch conflict
Option D:	Address conflict
5.	Which operation is performed in booth’s algorithm.
Option A:	Arithmetic left shift
Option B:	Logical left shift
Option C:	Arithmetic right shift
Option D:	Logical right shift

6.	The addressing mode used in an instruction of the form ADD AX , 07h is

Option A:	Direct
Option B:	Indirect
Option C:	Immediate
Option D:	Absolute
7.	In the memory hierarchy, as we go down the pyramid,
Option A:	Cost per bit decreases, Capacity increases, Access Time increases
Option B:	Cost per bit increases, Capacity decreases, Access Time decreases
Option C:	Cost per bit increases, Capacity increases, Access Time decreases
Option D:	Cost per bit decreases, Capacity decreases, Access Time decreases
8.	Each stage in pipelining should be completed within ___________ cycle.
Option A:	1
Option B:	2
Option C:	3
Option D:	4
9.	During execution of a program which register is initialized first?
Option A:	Instruction Register
Option B:	Program counter
Option C:	Memory address register
Option D:	Memory data register
10.	____________ is the raw material used as input and __________ is the processed data obtained as output of data processing.
Option A:	Data, Instructions
Option B:	Instructions, Program
Option C:	Data, Program
Option D:	Program, Code
11.	Arbitration does not fail when__________
Option A:	devices on the bus have logic errors
Option B:	manufacturing defects
Option C:	are driven beyond their design speeds
Option D:	more devices compete for the control of the bus
12.	Calculate biased exponent for 25.2 decimal to represent it in floating point single precision format.
Option A:	127
Option B:	128
Option C:	131
Option D:	133
13.	Represent (-35) decimal in 2's complement representation
Option A:	1100011
Option B:	1011101
Option C:	1011001
Option D:	1001111
14.	The method of mapping the consecutive memory blocks to consecutive cache

	blocks is called _______.
Option A:	Set associative
Option B:	Associative
Option C:	Direct
Option D:	Indirect
15.	Perform binary division 1110100 / 100
Option A:	11001
Option B:	11101
Option C:	11011
Option D:	11000
16.	Result of the division (7/3) by using restoring division algorithm is
Option A:	M = 0111, Q = 0001, A = 0010
Option B:	M = 0011, Q = 0010, A = 0001
Option C:	M = 0111, Q = 0010, A = 0001
Option D:	M = 1111, Q = 0010, A = 0001
17.	Which one of the following parameters is not a part of Computer Organization?
Option A:	Control signals
Option B:	Instruction set
Option C:	Memory interface techniques
Option D:	Activation of control signals
18.	To extend the connectivity of the processor bus we use
Option A:	PCI bus
Option B:	SCSI bus
Option C:	Controllers
Option D:	Multiple bus
19.	Which factor determines the effectiveness of the cache?
Option A:	Hit rate
Option B:	refresh cycle
Option C:	refresh rate
Option D:	refresh time
20.	Which factor determines the number of cache entries?
Option A:	set commutativity
Option B:	set associativity
Option C:	size of the cache
Option D:	number of caches

Q2. **(20 Marks)**	**Solve any Four out of Six.** **5 marks each**
A	Explain Booth's Algorithm. Perform multiplication of (-12 * 5) using booths algorithm.

B	Explain Von Neumann model. What is the role of different registers like IR, PC, MAR, MBR in Von Neumann model.
C	What is flip flop? Write truth table of SR, JK, D, T flip flop.
D	Explain instruction cycle with neat diagram.
E	What is bus arbitration? Explain types of bus arbitration.
F	Explain various pipeline hazards.

Q3. **(20 Marks)**	**Solve any Two Questions out of Three** **10 marks each**
A	Differentiate between hardwired and microprogrammed control unit and Explain Wilke's Microprogrammed control unit with neat diagram.
B	Consider a cache memory of 16 words. Each block consists of 4 words. Size of the main memory is 256 bytes. Draw associative mapping and Calculate TAG & WORD size.
C	Write short note on amdahl's law and Explain Flynn's classification.