Program: **Computer Engineering**
Curriculum Scheme: Rev2012
Examination: Second Year Semester III
Course Code: CSC304 and Course Name: Digital Logic Design and Analysis
Time: 1 hour Max. Marks: 50
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Note:- All the Questions are compulsory and carry equal marks .

Q1.	The given hexadecimal number (1E.53)16 is equivalent to _____
Option A:	(35.684)8
Option B:	(36.246)8
Option C:	(34.340)8
Option D:	(35.599)8
Q2.	The expression Y=AB+BC+AC shows the _____ operation.
Option A:	EX-OR
Option B:	SOP
Option C:	POS
Option D:	NOR
Q3.	A product term containing all K variables of the function in either complemented or uncomplemented form is called a _____
Option A:	Minterm
Option B:	Maxterm
Option C:	Midterm
Option D:	∑ term
Q4.	Full subtractor can designed using
Option A:	One half subtractor, two OR gates
Option B:	Two half subtractors, one OR gate
Option C:	Two half subtractors, two OR gates
Option D:	Two half subtractors, one AND gate
Q5.	Add the two BCD numbers: 1001 + 0100 = ?
Option A:	10101111
Option B:	01010000
Option C:	00010011
Option D:	00101011
Q6.	The decimal equivalent of the excess-3 number 110010100011.01110101 is _____
Option A:	970.42
Option B:	1253.75
Option C:	861.75
Option D:	1132.87
Q7.	For following boolean function- F(W, X, Y, Z) = Σm(1, 3, 4, 6, 9, 11, 12, 14) This function is independent _____ number of variables.

Option A:	5
Option B:	4
Option C:	3
Option D:	2
Q8.	Minimize the following boolean function- $F(A, B, C, D) = \Sigma m(0, 2, 8, 10, 14) + \Sigma d(5, 15)$
Option A:	ACD + B'D'
Option B:	ACD' + BD
Option C:	ACD' + B'D'
Option D:	ACD + BD
Q9.	MOD 5 asynchronous counter will require ____ flip flops and will count from 000 to _____.
Option A:	5,111
Option B:	5,100
Option C:	3,100
Option D:	3,101
Q10.	The minimum number of flip flop required for mod 10 ripple counter
Option A:	4
Option B:	12
Option C:	3
Option D:	6
Q11.	How many select lines would be required for an 8-line-to-1-line multiplexer?
Option A:	2
Option B:	3
Option C:	4
Option D:	8
Q12.	The main advantage of TTL is
Option A:	Higher fan in and fan out
Option B:	Fast switching and low power consumption
Option C:	Higher noise margin and low cost
Option D:	Low cost
Q13.	Recommended fan out for TTL gate is
Option A:	10
Option B:	4
Option C:	20
Option D:	50
Q14.	VHDL stands for
Option A:	very high-speed integrated circuit hardware description language
Option B:	very high-speed integrated circuit hardware data language
Option C:	very high-speed integrated circuit hard description language
Option D:	very high-signal integrated circuit hardware description language

Q15.	Library ieee;
	use ieee.std_logic_1164.all;
	
	entity circuit is
	port(a,c:in bit; d,b:out bit);
	end circuit;
	
	architecture data of circuit is
	begin
	d<= a xor c;
	b<= (a and (not c));
	end data;
	
	The above VHDL code is for…

Option A:	Full Adder
Option B:	Half Adder
Option C:	Half subtractor
Option D:	Full subtractor
Q16.	In Hamming code, The number of redundant bits can be calculated using the following formula:
Option A:	$2^r \geq m + r + 1$ where, r = redundant bit, m = data bit
Option B:	$2^m \geq m + r + 1$ where, r = redundant bit, m = data bit
Option C:	$2^1 \geq m + r + 1$ where, r = redundant bit, m = data bit
Option D:	$2^n \geq m + r + 1$ where, r = redundant bit, m = data bit
Q17.	What is the minimal Hamming distance between any two correct codewords?
Option A:	1
Option B:	2
Option C:	3
Option D:	4
Q18.	Simplify following Boolean expression (A+B) (A+C)
Option A:	A+B+C
Option B:	AB+C
Option C:	AC+B
Option D:	A+BC
Q19.	What is the difference between a ring shift counter and a Johnson shift counter?
Option A:	No difference
Option B:	A ring shift counter is faster
Option C:	feedback is reversed
Option D:	Johnson shift counter is faster

Q20.	For realization of SR flip-flop from JK flip-flop, if S=1, R=0 & present state is 0 then next state will be _____
Option A:	1
Option B:	0
Option C:	Don't care
Option D:	toggle
Q21.	Which one is not the outcome of magnitude comparator is _____
Option A:	A=B
Option B:	A>B
Option C:	A<B
Option D:	A-B
Q22.	In case of Decoder, when D4 is HIGH then input x,y,z has following values
Option A:	011
Option B:	100
Option C:	101
Option D:	110
Q23.	Which of the following expressions is in the product-of-sums form?
Option A:	(A + B)(C + D)
Option B:	(AB)(CD)
Option C:	AB(CD)
Option D:	AB + CD
Q24.	How many 2 : 1 MUX are required to implement 16 : 1 MUX.
Option A:	8
Option B:	15
Option C:	16
Option D:	17
Q25.	Gray code representation of 14 is
Option A:	1010
Option B:	1100
Option C:	1001
Option D:	1110