Program: **Computer Engineering**
Curriculum Scheme: Rev2016
Examination: Second Year Semester III
Course Code: CSC302 and Course Name: Digital Logic Design and Analysis
Time: 1 hour Max. Marks: 50
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Note:- All the Questions are compulsory and carry equal marks .

Q1.	The octal equivalent of 1100101.001010 is _____
Option A:	624.12
Option B:	145.12
Option C:	154.12
Option D:	145.21
Q2.	It is a single input version of J-K flipflop formed by trying both the inputs of J-K
Option A:	D Flipflop
Option B:	S Flipflop
Option C:	T Flipflop
Option D:	R Flipflop
Q3.	The output of Half adder is in the form of
Option A:	Sum
Option B:	Carry
Option C:	Sum and Carry
Option D:	Addition
Q4.	Full adder can designed using
Option A:	One half adder, two OR gates
Option B:	Two half adder, one OR gate
Option C:	Two half adder, two OR gates
Option D:	Two half adder, one AND gate
Q5.	The decimal number is converted in to excess 3 code by adding to each decimal digit.
Option A:	4
Option B:	8
Option C:	2
Option D:	3
Q6.	Hexadecimal Addition of (3A5)16 and (1B2)16 will give :
Option A:	557
Option B:	185
Option C:	815
Option D:	516
Q7.	Which of the examples below expresses the commutative law of multiplication?
Option A:	A + B = B + A
Option B:	A • B = B + A

Option C:	A • (B • C) = (A • B) • C
Option D:	A • B = B • A
Q8.	Minimize the following boolean function- $F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$
Option A:	B'D + B'C' + A'D'
Option B:	B'D + B'C'
Option C:	AD + B'D + B'C' + A'D'
Option D:	AD + B'D + B'C'
Q9.	MOD 6 asynchronous counter will require ____ flip flops and will count from 000 to _____.
Option A:	6,101
Option B:	6,110
Option C:	3,110
Option D:	3,101
Q10.	The minimum number of flip flop required for mod 12 ripple counter
Option A:	4
Option B:	12
Option C:	3
Option D:	6
Q11.	How many select lines would be required for an 16-line-to-1-line multiplexer?
Option A:	2
Option B:	3
Option C:	4
Option D:	16
Q12.	If a logic circuit has a fan out of 4 then the circuit ….
Option A:	Has 4 inputs
Option B:	Has 4 output
Option C:	Can drive maximum of 4 inputs
Option D:	Gives output 4 times the input
Q13.	Which of the following logic family dissipates minimum power?
Option A:	CMOS
Option B:	ECL
Option C:	TTL
Option D:	DTL
Q14.	VHDL stands for
Option A:	very high-speed integrated circuit hardware description language
Option B:	very high-speed integrated circuit hardware data language
Option C:	very high-speed integrated circuit hard description language
Option D:	very high-signal integrated circuit hardware description language

Q15.	Library ieee;
	use ieee.std_logic_1164.all;
	
	entity adder is
	  port(a,b:in bit; sum,carry:out bit);
	end adder;
	
	architecture data of adder is
	begin
	  sum<= a xor b;
	  carry <= a and b;
	end data;
	
	The above VHDL code is for…

Option A:	Full Adder
Option B:	Half Adder
Option C:	Half subtractor
Option D:	Full subtractor
Q16.	In Hamming code, Suppose the number of data bits is 7, then the number of redundant bits required is_____and total bits is_____
Option A:	3,10
Option B:	4,11
Option C:	5,12
Option D:	6,13
Q17.	Which of the following is/are the universal logic gates?
Option A:	OR and NOR
Option B:	AND
Option C:	NAND and NOR
Option D:	NOT
Q18.	Simplify following Boolean expression (A+B) (A+C)
Option A:	A+B+C
Option B:	AB+C
Option C:	AC+B
Option D:	A+BC
Q19.	What is the difference between a ring shift counter and a Johnson shift counter?
Option A:	No difference
Option B:	A ring shift counter is faster
Option C:	feedback is reversed
Option D:	Johnson shift counter is faster
Q20.	For realization of SR flip-flop from JK flip-flop, if S=1, R=0 & present state is 0 then next state will be _____

Option A:	1
Option B:	0
Option C:	Don’t care
Option D:	toggle
Q21.	In 1 bit Magnitude comparator, if A=1 and B=0 then which output will be set to 1
Option A:	A=B
Option B:	A>B
Option C:	A<B
Option D:	None of the above
Q22.	In case of Decoder, when D4 is HIGH then input x,y,z has following values
Option A:	011
Option B:	100
Option C:	101
Option D:	110
Q23.	Which of the following expressions is in the product-of-sums form?
Option A:	(A + B)(C + D)
Option B:	(AB)(CD)
Option C:	AB(CD)
Option D:	AB + CD
Q24.	How many 2 : 1 MUX are required to implement 8 : 1 MUX.
Option A:	5
Option B:	6
Option C:	7
Option D:	8
Q25.	Gray code representation of 14 is
Option A:	1010
Option B:	1100
Option C:	1001
Option D:	1110